Improved Accuracy and Runtime of IC Power Supply Noise Simulations through Multi-Phase and Voltage Controlled Resistor Analyses

2010-2011 Micron Clinic Team:
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***Abstract*- As Integrated Circuits have become more complex, having more, smaller, transistors, accurate SPICE simulation of these devices has become harder to perform. There have been multiple commercial attempts to solve this problem, but none reproduce the accuracy of the industry standard HSpice. This project experiments with two new simulation strategies: Multi-Phase analysis and Voltage Controlled Resistor (VCR) substitution. Multi-Phase analysis is based on current commercially available simulators, but extends the same idea in expectation that it will converge to some value. VCR substitution seeks to replace complex circuit structures in simulation with a model that may be less computationally demanding.**

I. Project Motivation

As modern technology continues to evolve, one of the most important driving elements behind new innovation is the ability, through Integrated Circuits (ICs), to put more electronic functionality into a smaller area. As technology improves, the size of transistors that ICs are made of get smaller as well, allowing for the same functionality in a smaller area or greater functionality in the same area. As an example, consider the DRAM used in modern computers. Average computers these days come with 2-4GB of DRAM. In 1GB of DRAM, not including the encoding hardware, there are over one billion transistors. As technology improves even more of them are placed in one single circuit, making it ever more complex.

While the transistors are getting smaller the clock frequencies at which they run have been driven higher. This presents a problem as the components that comprise the Power Delivery Network (PDN) are also necessarily getting smaller to match the rest of the circuit, which means that it has a higher resistance. This higher resistance limits the PDN's ability to provide a constant voltage to the IC due to demands in the current through the transistors during switching at the new, higher, frequencies.

This problem is further complicated by the fact that an IC must be placed in a package of some sort to integrate it with the larger system that it works with. The package, due to unavoidable limitations in design, adds further resistance as well as other types of impedances to the PDN. The combination of the package and the smaller size makes for a noisy supply voltage where a perfect DC voltage is ideal.

The transients that result from the combinations of the before mentioned problems were not as big of a problem in the past, because ICs used a high enough power supply voltage that they were relatively small. Another thing that has gotten smaller as transistors have become smaller is the depth of the gate oxide. If the gate oxide is thinner it can't stand the higher voltages that older technologies could handle, so extremely large voltage transients can be dangerous to the device.

The basis of experimentation in this project is IBM's 65nm 10sf process that runs on a power supply of 1.2V. This is much lower than, for instance, the common 5V power supply of a slightly older technology. By comparison a seemingly small voltage swing, 0.5V for example, is a much larger percentage of the total supply voltage at 1.2V than the same swing at a 5V supply. The supply voltage level plays an important role in the function of the circuit, and the speed at which it can operate.

The true motivation for this project comes from the problems that can come from PDN noise. Due to the addition of more components to a circuit it becomes more complex, which makes it harder to run SPICE simulations on. During the design process there is really no way to manually calculate what the behavior of PDN as a result of what is happening in the circuit, so the best alternative is to use computer based SPICE simulations to see how they perform. A problem lies in the fact that the industry's "gold standard" [1] for circuit verification and analysis, HSpice, takes a very long time to simulate a very complex circuit, if it can finish the simulation at all. This lends to the need for other types of simulation methods that will produce results that are accurate enough to give the circuit designer the information needed about the performance of the PDN and by extension the rest of the circuit.

II. Project Description

The project as proposed by the sponsor, Micron Technology, is, in short, to experiment with various methods of SPICE simulation currently on the commercial market, as well as some new methods, and see which ones prove viable as replacements for HSpice or as a tool to be used in conjunction with HSpice when a faster verification is required. The methods proposed to compare are the current "gold standard," the commercially available "Two-Phase" strategy, a Multi-Phase analysis, and a Voltage Controlled Resistor substitution method.

The project in its inception was planned to take two years to complete. The first year of the project was during the 2009-2010 school year. That team built the circuits which would be simulated to collect data and experimented with the commercially available simulator alternative HSIM^{plus}. The second year was the 2010-2011 school year. That team experimented with the new simulation strategies of Multi-Phase analysis, and the VCR substitution model. These new simulation strategies will be the topic of this report.

The idea behind the Multi-Phase analysis is similar to the two-phase approach taken in HSIM^{plus}. The idea is that parts of the overall circuit can be taken out of the circuit and simulated quickly individually to see what sort of behavior they have with regards to the overall circuit function. These parts are then included in the larger simulation as a current source that draws current from the power rails in a way that mimics what the original circuitry did under the circumstances of the simulation. This two-phase analysis can be summed up into the two phases:

1. Simulate smaller blocks of circuitry to determine their current draw throughout the simulation.
2. Replace those blocks in the PDN with current sources and simulate the behavior of all parts.

The Multi-Phase analysis extends this process to get better accuracy. Where the two-phase model stops after the second simulation step, the Multi-Phase approach takes the effects of the current drawn from the power rails, as a noisy voltage, and applies them back to the smaller circuit blocks as the new power rail. This would only be considered three phases, but the methodology is open ended and can be repeated as many times as a user has patience to do it. Eventually these simulations should converge on some signal for the PDN which should be equivalent to what HSpice would produce, but in a shorter time period, assuming the repetition of steps isn't done so many times that it takes as long as the original simulation.

The idea behind the VCR model is to perform something similar to the two-phase approach, but rather than replacing the smaller circuit blocks with current sources, replace them with VCRs. The idea here is that a VCR will allow the noise on the power supply to effect the current flowing through the PDN model, resulting in a more accurate representation of the power supply noise. Currently the current source used in the two-phase model gives an overestimation of the power supply noise. This is because the current source does not allow the power supply noise to effect the current flowing through the PDN. The thought here is that the less computationally demanding model could make the simulation potentially equally as accurate, while being faster than a full HSpice simulation.

III. Methods

A. Tool Design

HSpice is the most logical simulator to use for this project because it is so widely used in industry. This means that its behavior and output types are very well known. The benefits of the thorough knowledge of HSpice output types are that it is well known where to find the data that is needed for the next simulation and that there are tools available to handle some of the output types. In the end though, HSpice was used because of the mentality that these new methods are hoping to achieve HSpice accuracy in a way that is faster, so it makes more sense to base the new methods on the most accurate simulation method we can come up with.

The overarching need for this project (both Multi-Phase and VCR analyses) is a method of quickly formatting data from one simulation in such a way that it can be used in another. For this purpose scripts are necessary to extract and apply the simulation as well as control the surrounding processes that create, modify, and format the information. Perl seems to be the best scripting language to use for the processes in this project because of its capability to manipulate data in the form of text files.

The fact that adding a package model to the simulation of an integrated circuit gives the most significant increase in simulation time of any accuracy added [1] makes it the primary focus for this project. If the package model can be removed from the large complex circuit (henceforth referred to as the die), the simulation time drops significantly. This is where both simulation methods begin. Initially the circuit models are removed from the package model in the .control files that govern the behavior of the SPICE simulations. This gives the two parts for the analyses. Both the Multi-Phase approach and the VCR method are separated in this way but what is done with the two parts varies.

After the package model and the die are separated, the various simulations from which to extract data can be performed. For the Multi-Phase and the VCR the initial part of the process is to run an HSpice simulation of the .control file for the die. HSpice prints its output data in two ways as defined in the .control file.

The first data output file is a binary file which contains data from all nodes within the circuit being simulated. It is the .tr0 file. From this file the various waveforms can be viewed using various tools such as Cosmoscope, which is available on the machines in the Computer Aided Drafting and Engineering (CADE) lab on the University of Utah campus.

The second method contains data from all parts of the simulation; from initial conditions to total simulation time. This file can be commanded in the .control file to store all data points of a specified signal as a text table. This is the

.lis file. Although there are tools available for extracting information from the .tr0 file, the .lis approach proved to be the better source of the information in the end due to the fact that the tools for the .tr0 file don't give as high of a resolution on the waveforms as can be accomplished using the .lis file. For the sake of scriptability, the signals that information is required from are uniformly named in the .control files for the different parts of the simulation processes. Since the signals of concern for the scope of this project are the power and ground rail voltages, this is fairly easy to accomplish.

The first thing that the scripts do is run an HSpice simulation on the die .control file specified as an input to the script. After this simulation is complete the specified signals are available in the .lis file. The script sorts through the information in the .lis file until it finds the first signal; and stores its data into an array. It proceeds through the .lis file until it finds the second signal and stores this information into a second array. From here the scripting varies between the two simulation methods.

For the Multi-Phase method it is not necessary to change formatting of the data points since the only program of concern is HSpice, and it uses the same formatting on inputs as it outputs. The arrays of data are combined with an array of time steps from the same source. These arrays will be used to create a piecewise-linear current source that will be connected into the package model in place of a dummy model that is already implemented in the package .control file on the power and ground nets. After the arrays are created the script opens the .control file for the package model an sorts through it until it finds the first source that will be replaced and then prints out the formatting required for the piecewise linear source that will simulate the die. It continues until it finds the second source and replaces it. After the sources are implemented a simulation is run on this new .control file with the current sources in place. When this simulation completes, the process repeats itself except it is getting voltage data from the power and ground nets and inputting them as piecewise linear voltage sources as the power supply rails in a simulation set up for the die. This is where the script stops leaving it up to the user to continue through and make it a multi-phase analysis rather than a two-phase. The script can be restarted with the new die .control file and run through another iteration of the process. The data points can be saved along the way for comparison with the ideal case of the circuit setup in HSpice and other analysis methods.

The major difference with the VCR method is that the data in the arrays of the current information has to be formatted for use in other calculations before it can be turned into a piecewise linear source. The problem with the data in the state that it comes out of the .lis file is that it is in SPICE format, so instead of exponents it has the symbols for exponents (i.e. u, p, m, etc.). This must be changed into an actual exponent value before calculations

can be done on these numbers so that the control voltage sources on the VCRs can be created. The script goes through the arrays of current data and creates a new array of properly formatted current data. This data is written out to a file where it waits until the Perl script initiates MATLAB to run a script. The MATLAB script reads in the current data, does the necessary calculations on it, formats the output of the data and writes it out to new files from which the Perl script can use it. These files are opened, parsed, and their data is stored into formatted arrays for putting into a .control file. After these are created the script searches through the package model .control file until it locates the dummy control voltage sources. It then replaces them with piecewise linear voltage sources that make them duplicate the current drawn by the circuit it is simulating. After these sources are in place one final simulation is run and the output of it can be viewed and compared.

B. Multi-Phase Analysis

Micron has supplied our team with a 'black box' circuit package that includes many of the internal impedances, capacitances, and resistances of a real-world circuit package. Last year's team provided the circuits that we are using for this year's project; a 4-inverter circuit, a 16-bit adder, an 8-bit multiplier, a 4-stage Fibonacci circuit (utilizing a 16-bit adder for each stage), an 8-stage Fibonacci circuit, and a 16-stage Fibonacci circuit. Our approach was not to tackle the internal workings of the software itself and change the two-pass (or two-phase) method, but rather to simplify the circuit by separating the circuit into two separate pieces; the die (internal circuit) and the package (see Figure 1 below).

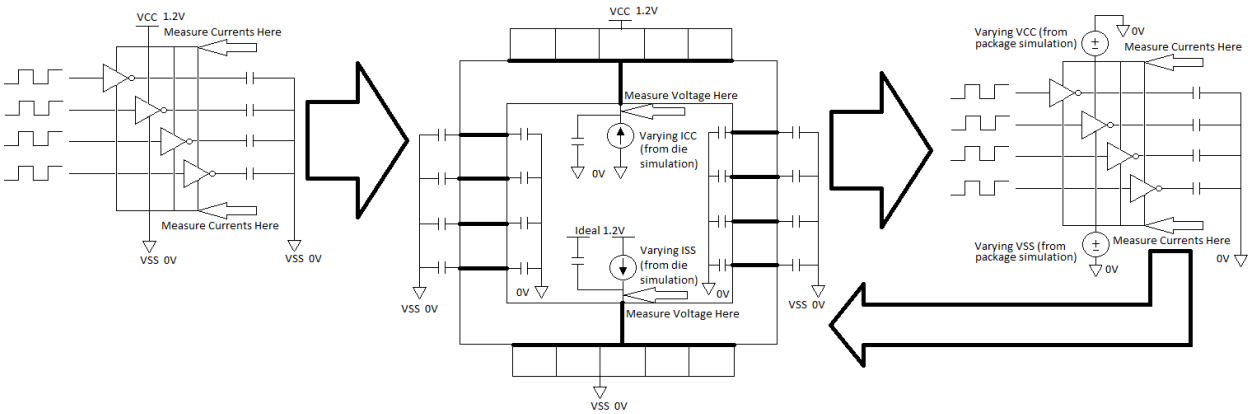

Figure 1 – Multi-Phase Method
NOTE: The third stage replaces the first during the 2nd (and consecutive) iteration(s)

The flow diagram in Figure 1 shows the need for multiple circuits to be designed for the Multi-phase approach. The circuits needed for building and simulating the Multi-Phase approach are as follows:

- Baseline Circuits, for standard HSpice and HSIM^{plus} simulation comparisons of Multi-Phase outputs
- Die (internal circuit), first phase of the Multi-Phase method
- Package Model, second phase of the Multi-Phase method

The first circuit to be designed was the baseline circuit. These circuits originally used at the onset of this project were designed and used by last year's team for their purposes and results. We decided not to modify the circuits, in order to see where our results for the Multi-Phase approach compared against. Each of the circuit models that we proposed to analyze needed to have a separate baseline model created, but each will have the same basic configuration that we have developed for the 4-inverter circuit. See Figure 2 for the original circuit model of the 4-inverter circuit model; not all of the nodes are fully represented.

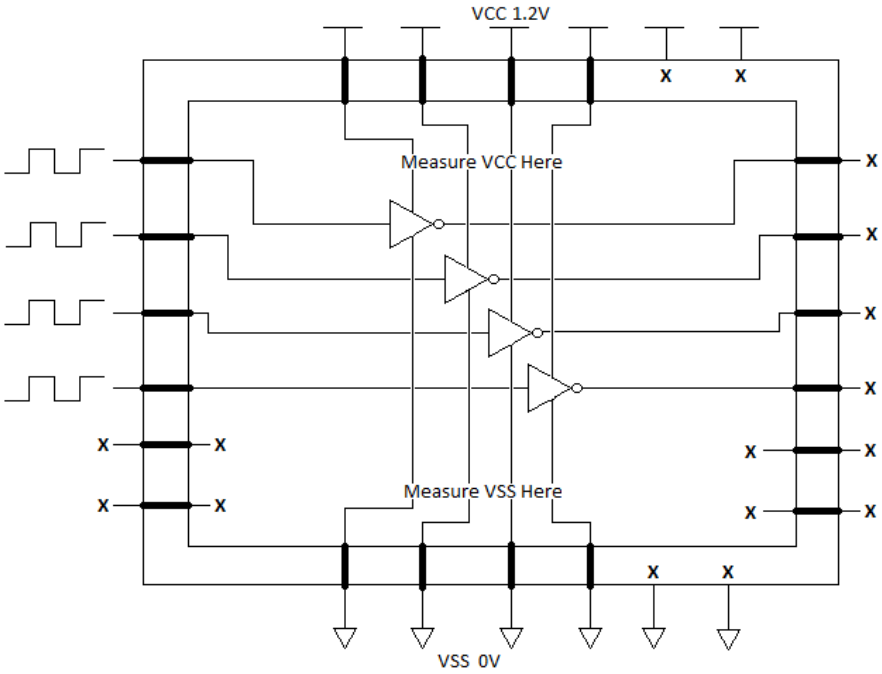

Figure 2 – Original Simulation Setup as Determined by Last Year's Team

For the baseline model, the die is inside the package model with the signals propagating through the package to the inputs of the die. The output signals of the die are then propagated back through the package model. The power (VCC) pins, as well as the ground pins (VSS), propagated through the package individually to the power and ground pins on the die. No terminals had any capacitance values on either the exterior or interior of the design. This capacitance problem would be corrected later on in the project as there was a need for real-world placement within

larger designs, causing these circuits to be connected to loads and also to minimize the effects of mutual inductance on terminals with no load connections.

The second circuit to be designed was the internal circuit only, the die. The baseline circuit was modified by removing the package completely so that only the circuit die remained (see Figure 1 Phase 1 for the 4-inverter representation of this circuit). The power to the die was supplied with a single ideal voltage source connected to all of the power pins of the inverters that supplies a steady 1.2 volts. The ground to the die was a voltage source connected to all of the ground pins of the inverters that supplies an ideal 0 volts to be an artificial ground. We need an artificial ground in order to see the ground rail currents during operation of the circuit. These voltage supplies are replaced after the second phase of the Multi-Phase simulation has been completed as discussed in the scripting method above. Initially there were no loads connected to the output pins of the inverters because there were not any terminations on the output pins of the original baseline circuit. Later, capacitor loads were placed on each of the output pins to better simulate real-world signal propagation of the baseline output waveform.

The third circuit to be designed was a package circuit without the die. The baseline circuit was modified again to remove the die out of the package model and place two piece-wise linear (PWL) current sources inside the package that would represent the currents drawn by the die circuit during the first phase simulation on the power node and ground node. Originally, the signal pins remained but were later removed because it was noticed that they created a duplicate input waveform with delay and magnitude differences because of the mutual inductances introduced by the package model. See Figure 1 (Phase 2) for the modified package model without the 4-inverter die.

After performing many simulations of the initial Multi-Phase approach, the output waveforms were, predictably, not responding to the signal stimulation in either the standard simulation of the baseline model or the Multi-Phase simulation regardless of the myriad of revisions made to the Multi-Phase circuit model. It became apparent that modifications of the original baseline model needed to be performed. Notice the unterminated inputs, outputs, power, and ground pins in Figure 2. The package model provided by Micron is extremely complicated with many mutual inductances, capacitances and resistances. The mapping of the single-layer package was provided to us by last year's team which was a very complicated process because of the proprietary nature of the package model. There are several extra pins on the exterior of the package compared to the interior; several pins on the outside of the package are connected to a single interior pin. The unpredictability of the unterminated wires was too large, therefore it was decided to place 2pF loads on each side of the unused signal pins. It was also necessary to tie all of the power pins together and the ground pins both on the inside and on the outside of the package model. Another

modification needed was a capacitive replacement of the die. The die itself has an inherent coupling capacitance and the transistors within the circuit have parasitic capacitance associated with each of them. That capacitive network was replaced by a coupling capacitor on the ground pin and the power pin. See Figure 3 for the revised baseline model.

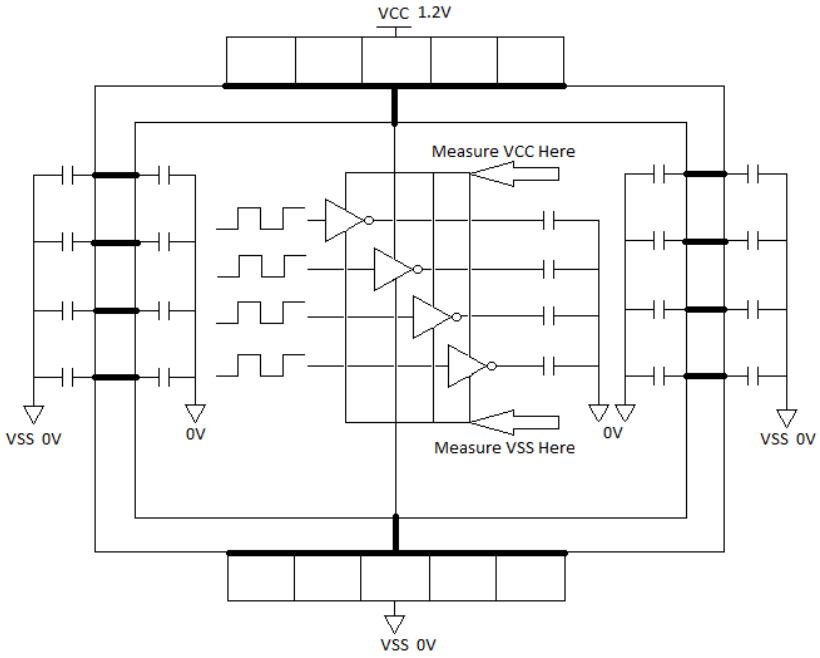

Figure 3 – Revised Baseline HSpice Simulation Method

With the smaller circuits that were simulated (4-inverter circuit, 8-bit multiplier, and the 16-bit adder), there was not a significant difference between the revised version of the baseline circuit and the revised circuit of the Multi-Phase analysis using the coupling capacitance with the power and ground rails. As the Fibonacci circuits were being simulated, the difference became apparent (see Multi-Phase results section below for further explanation and output waveforms) that there needed to be more filtering occurring before the power and ground rail response would represent the behavior of the baseline simulation response. The final Multi-Phase revision needed to be developed. There needed to be some method of circuit replacement that would more accurately represent the capacitive, resistive, and inductive elements of the circuit being replaced. Trying to develop a singular filter circuit that would model the missing circuit with the capability of hundreds to thousands of transistors would be a monumental task to undertake. Therefore the removed circuit would be placed back into the package model with all of the inputs and outputs tied to capacitors (see Figure 4). It would not respond except to create missing capacitive, resistive, and inductive elements even though they would not be switching to exactly represent the baseline model, it would help the Multi-Phase results more closely represent the output waveform of the baseline model. This method of circuit

replacement in the second phase of the Multi-Phase approach would be the standard Multi-Phase method of analysis for all of the simulated circuits.

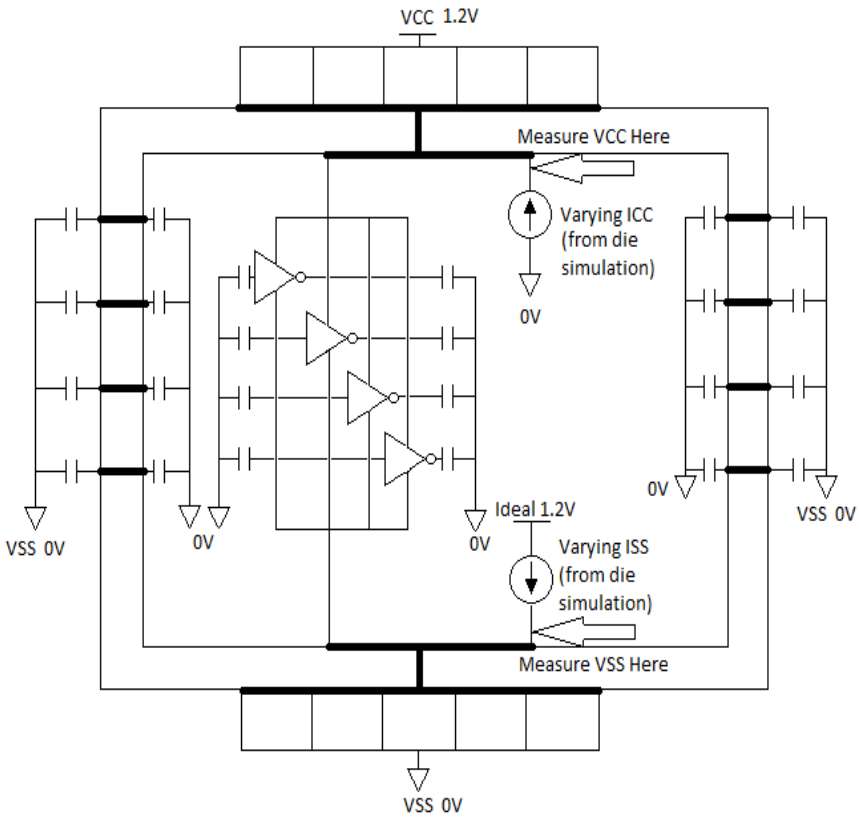

Figure 4 - Removed Die is Replaced, Second Phase of Multi-Phase Method Shown in Figure 1

C. Voltage Controlled Resistor Function

Noise on the power supply will affect the current flowing through a circuit. Normally as noise causes the power supply voltage to drop, the current in the circuit would decrease, thus limiting the drop in supply voltage. However, when a current source is used to set the current in the circuit, the supply noise will not affect the current draw. This leads to an overestimation of the supply noise. Using a VCR to create these currents instead of a current source would allow the power supply noise to affect the current flowing through the circuit. By using a VCR instead of a current source, a more accurate representation of power supply noise is anticipated. Also because of the simple equations that govern the VCR, it is expected that simulation times will remain shorter than a complete HSpice simulation.

i. VCR Model

Several different VCR models were found in addition to the native Spice VCR model, however, only two of them worked with the version of HSpice available in the CADE lab. Both working models were found

to have similar performance. It was decided to use the non-native model in our simulations. The VCR model used for simulations is shown in Figure 5. It works by measuring the current flowing through the VCR using the V_{SENSE} source. This current is then forced across reference resistor R_{RES} by a current source F_{COPY}. The voltage drop across R_{RES} is then scaled by the Control voltage present across nodes four and five. The voltage source E_{RES} takes the value of this scaled voltage, which results in a voltage drop across the VCR [3]. The value of this voltage drop is given by equation (1), where I is the current flowing through the VCR and V_C is the control voltage.

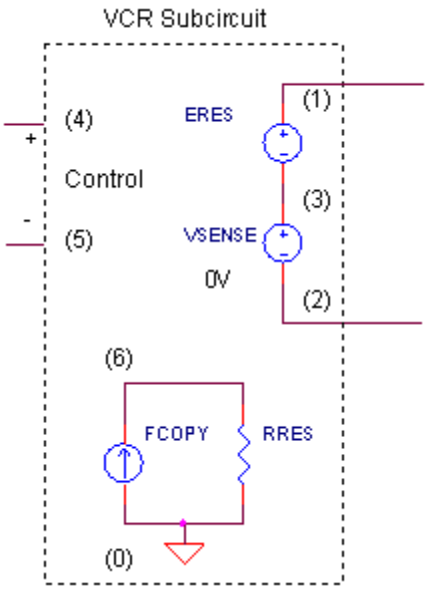

Figure 5 - VCR sub-circuit model. [3]

$$V = I \cdot RRES \cdot Vc \tag{1}$$

After verifying that the VCR model was working properly, the next step in integrating the VCR into the two-phase analysis was to design a circuit that would use the VCR to reproduce currents.

ii. Current Generation Circuit

To be able to replace the current sources in the two-phase model, the VCR must be capable of accurately reproducing current waveforms. To test the current reproducing abilities of the VCR, a simple circuit that consisted of a VCR with one terminal tied to a power supply and the other tied to ground was designed. However, upon testing it was found that a resistor needed to be added in series with the VCR to provide the

circuit with a “real” resistance that would limit current flow. Figure 6 shows the current generation circuit with the added series resistor.

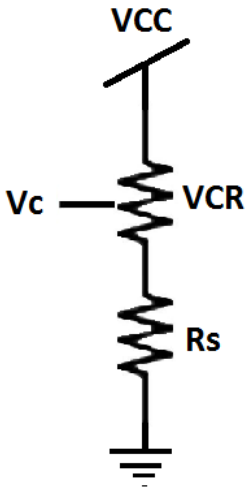

Figure 6 - VCR current generation circuit.

The current generating circuit was simulated with a varying control voltage and the resulting current waveform was observed. Figure 7 shows the current flowing through the circuit and the applied control voltage. From Figure 7 it can be seen that as the control voltage increases, corresponding to an increasing resistance, the current in the circuit decreases. Also as the control voltage decreases, the current increases. This verified that the current in the circuit could be altered using the VCR.

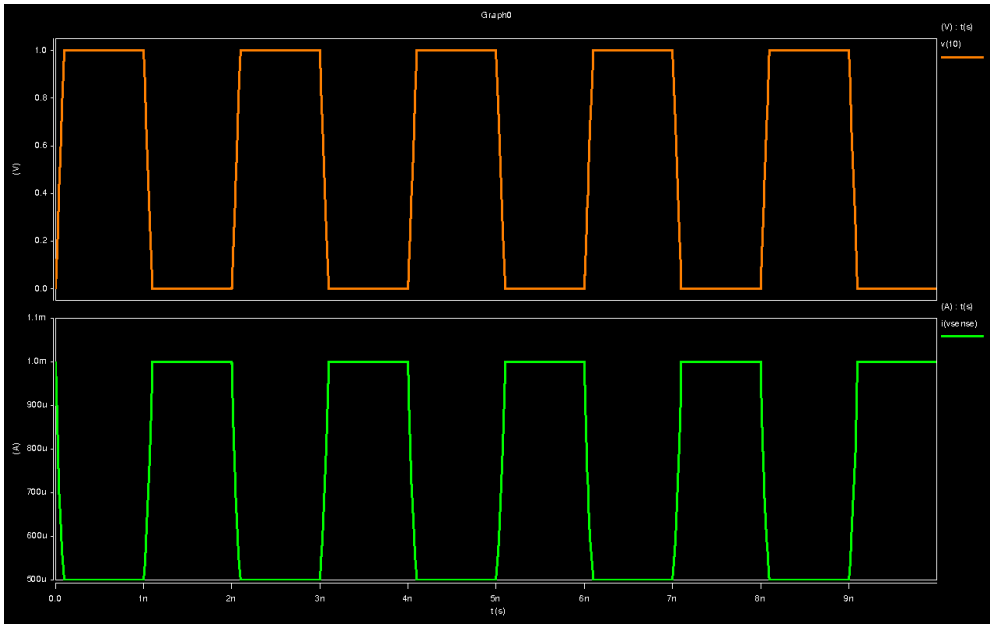

Figure 7 - Applied Control Voltage (Orange) and the Resulting Current (Green)

However, when trying to reproduce a given current waveform this circuit will not work. This is because the voltage drop across the VCR is dependent upon the current in the circuit. Thus we would be trying to use a dependent source to set the value that the source is dependent upon, which will not work. To fix this problem we notice that the VCR model is trying to mimic the voltage drop that is created by a resistor. Based on this observation the VCR model was changed such that F_{COPY} was set to a constant value of 1A and R_{RES} was set to a value of 1Ω, thus giving a constant voltage drop of 1V. Now the VCR model is no longer dependent upon the current flowing through it, and the voltage drop across the VCR is given by equation (2).

$$V = 1 \cdot Vc \tag{2}$$

To recreate a current waveform a MATLAB script is used to translate the current values into control voltage values for the VCR. From simple circuit analysis techniques, equation (3) was derived to be used by the MATLAB script, where I_d is the desired current value determined by the waveform to be recreated, VCC is the power supply voltage (1.2V for the 65nm technology we are using), and Rs is the resistor in series with the VCR. By using the ideal power supply value of 1.2V in the current-to-voltage equation this allows the power supply noise to affect the current in the circuit. If the power supply is at the ideal value, then VCR should produce a current value that is the same as the desired current waveform. However, if noise causes the power supply to change, the VCR will still have a resistance that would produce the desired current given an ideal supply; therefore the resulting current in the circuit would be higher or lower, depending on the change on the power supply.

$$Vc = VCC - (Id \cdot Rs) \tag{3}$$

D. Voltage Controlled Resistor Implementation

In order to investigate whether or not a two-phase analysis with the VCR is viable, a simulation method that uses a voltage controlled resistor will need to be used. The actual VCR setup will have two separate VCRs to model the power and ground voltages and currents separately. The resistor and capacitor were changed to different values. Most of the initial simulations the values of the resistor and capacitor were 1 kΩ and 100 pF respectively. The resistor value affects the control voltage by the current translation equation. The initial VCR circuit configuration is depicted in Figure 8.

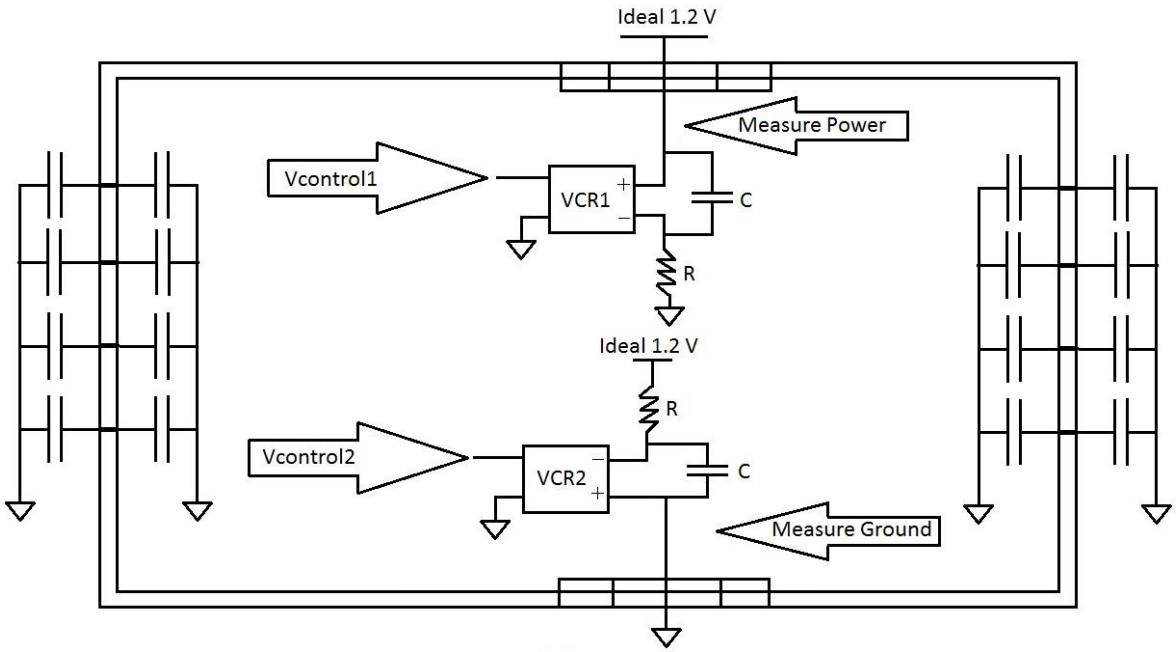

Figure 8 - Schematic of Two-Phase VCR Circuit

The first VCR (VCR1) is to model the power voltage response of the circuit being simulated. The second VCR (VCR2) shown is to model the ground voltage response of the circuit being modeled. The VCRs are connected inside a single layer package PDN. This is done in order to correctly model how the voltages and currents will react under the non-ideal power voltages created inside the package. The non-ideal voltages are created because of the parasitic components that model the single layer package.

As more of the circuit simulations were completed, the waveforms were not matching up with the HSpice baseline simulations. It became more apparent that the single capacitance will not replace the capacitance of the entire circuit being simulated. In order to better match the circuit's capacitance, a substitution of the entire circuit into the VCR configuration was used with the inputs and outputs capped off with 2 pF capacitors. The revised VCR configuration is shown in Figure 9.

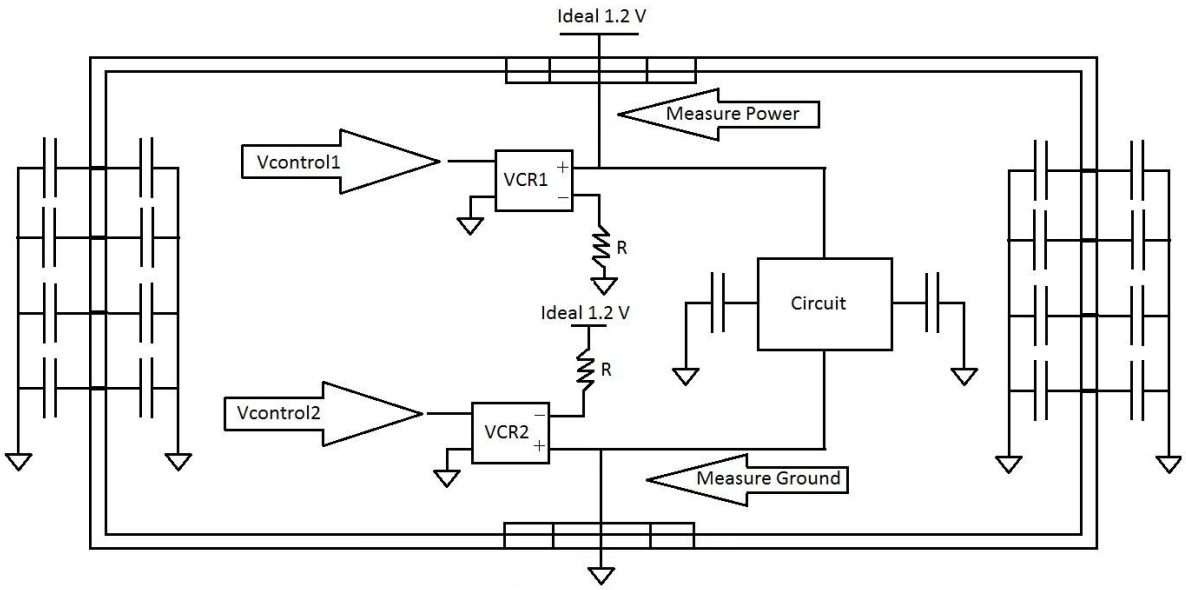

Figure 9 - Schematic of Revised VCR circuit

The revised configuration provided more accurate results when compared with results of the previous configuration, but there was a problem with both configurations. The problem was that the 4-inverter and 16-bit Adder results didn't match up well with their baseline simulations. The VCC voltage would be doing the opposite of what was intended. In order to correct this, further modifications were found to match up better. For the 4-inverter circuit the modifications that had to be made were that the positive and negative connections of both VCRs had to be switched to compensate for the differences with the HSpice baseline simulation. The change is shown in Figure 10:

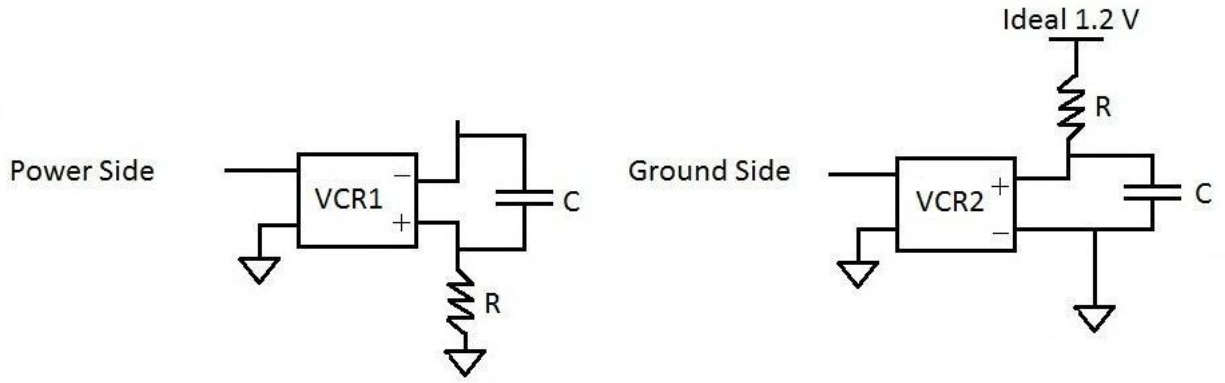

Figure 10 - Inverter VCR modification

With all three Fibonacci circuits and the adder circuit, the modification needed was to switch the polarity of VCR2. This is not a practical setup for the circuit with each individual modification. A single configuration that

works for all circuits will have to be found. The first attempt at finding this configuration was by decreasing the size of the resistor so that when converting the current into a control voltage, it would be all positive voltage. Since the control voltage on the VCR was setup as differential inputs, an experiment was tried by connecting the control voltage to the negative terminal and ground the positive terminal. In this setup the largely negative control voltage would be inverted due to the positive terminal being grounded. With a smaller resistor the control voltage would be largely positive and the control voltage terminals wouldn't need to be changed. The resistor value that was found to work in this situation was 10 Ω.

The results from this adjustment were an improvement, but the 4-inverter and 16-bit Adder circuits' results were not any closer to their HSpice baseline simulations, so that change ultimately didn't work out. In order to find the single configuration, examination of the control voltages was done to determine which one was exactly affecting the VCC voltage. It was discovered that VCR1 was affecting the wave spikes that were opposite of what the baseline simulations were. The new single configuration that was found to be able to use for all circuits is shown in Figure 11.

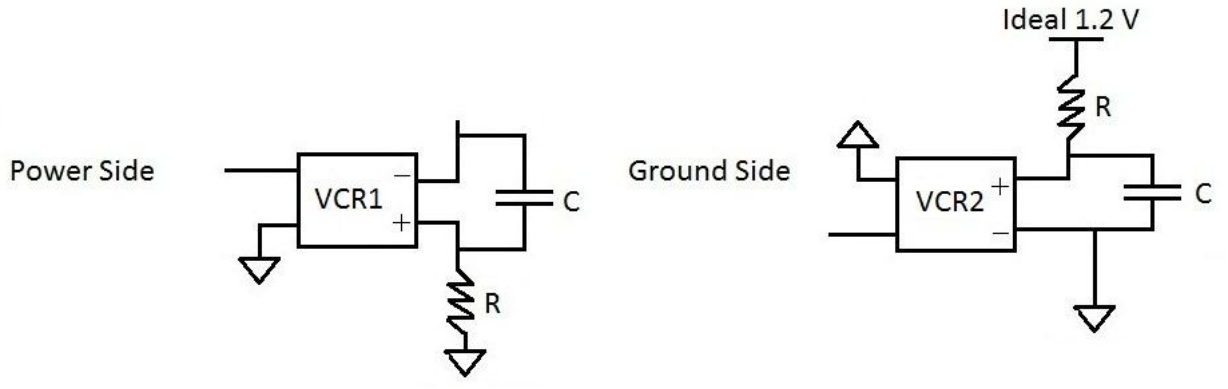

Figure 11 - New universal VCR circuit

The purpose for switching the inputs on the differential side was to offset the large negative control voltage being sent in. The large negative control voltage was created due to the resistor value of 1 kΩ. With this new setup, the results were more consistent with HSpice baseline simulations.

IV. Results

A. Multi-Phase Analysis

The goal of the Multi-Phase approach was to design a method to which the output would be close to the golden standard, HSpice. Over 60 simulations of multiple iterations were performed of the Multi-Phase approach. In all of these, the Multi-Phase simulation was tweaked slightly in all of them to determine how the circuit reacts to different

component values and component configuration changes. It was decided after all of the initial analysis that a modification to the baseline circuit was necessary. Figure 12 shows that the circuit was not responding to the input signals at all but was resonating from internal package filtering. The baseline circuit needed to be modified to simplify the inputs and outputs by terminating unused pins and connect all power and ground sources together. This would allow a more controlled separation of the baseline circuit into each of the circuits for the Multi-Phase approach as described in the methods section above.

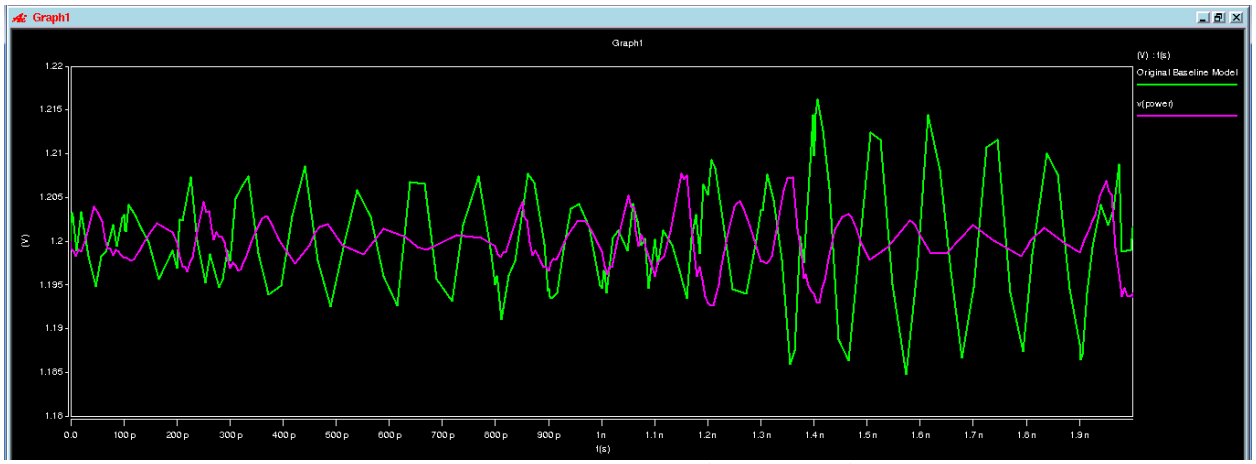

Figure 12 – Original Baseline Model (Green), 1st iteration of Multi-Phase of Original Circuit (Purple)

The four signal input waveforms to the inverters were staged and each initiated at 0 ps (picoseconds), 200 ps, 800 ps, and 1000 ps, with a 2000 ps cycle-time (See Figure 13). Figure 14 shows the original baseline model output response (purple) compared to that of the revised baseline model output response (green).

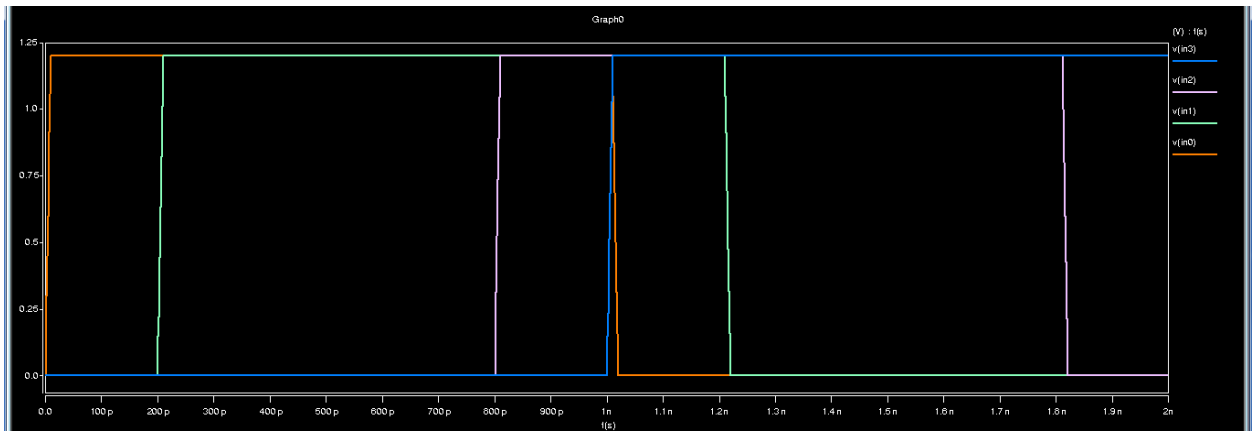

Figure 103 – Signal Inputs to 4-inverter Circuit

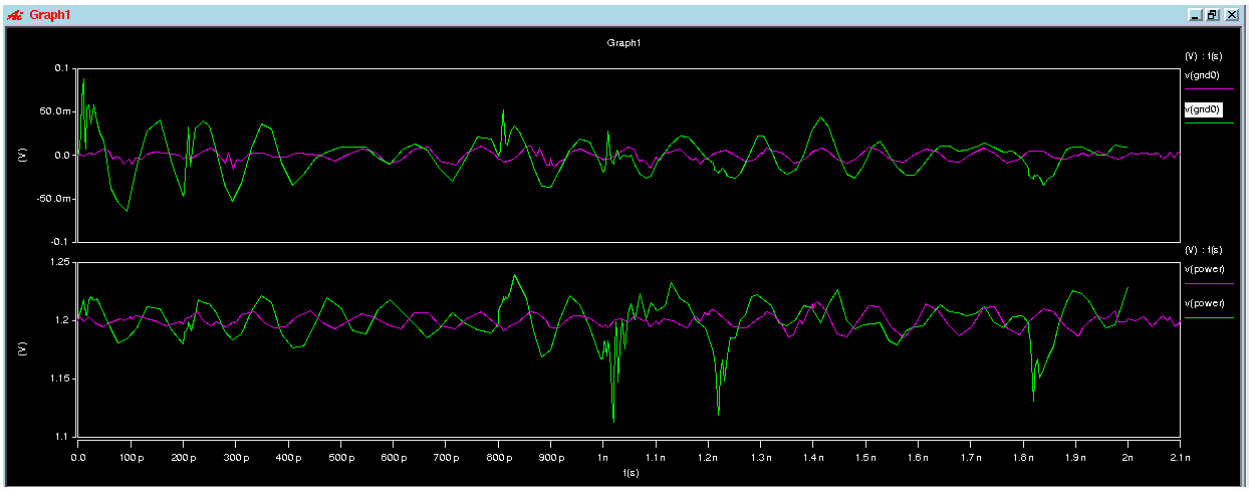

Figure 114 – Baseline HSpice Simulation (Purple), Revised Baseline HSpice Simulation (Green)

The input variations can be better seen in the revised waveform since it is now driving a capacitive load and has a better defined input waveform rather than a distorted waveform after being propagated through the package model. The reason that v(power) and v(gnd0) in Figure 14 vary so much at 1000 ps is because two signals are switching (one high and one low) simultaneously.

After establishing the baseline circuit, a comparison of the baseline (purple) and first iteration of the Multi-Phase (green) waveforms is compared as shown below in Figure 15.**Error! Reference source not found.** As evident, the noise on the power and ground rail are responding according to the variations occurring at the appropriate times as the inverters are switching. However, magnitudes of these waveforms are too large compared to the baseline waveform. It was decided that there was a missing capacitive element within the circuit. The die that is removed from the circuit has several capacitive values to be considered, the most notable of these is the coupling capacitance and the parasitic capacitances. This explains at least some of the effect of the differing waveforms.

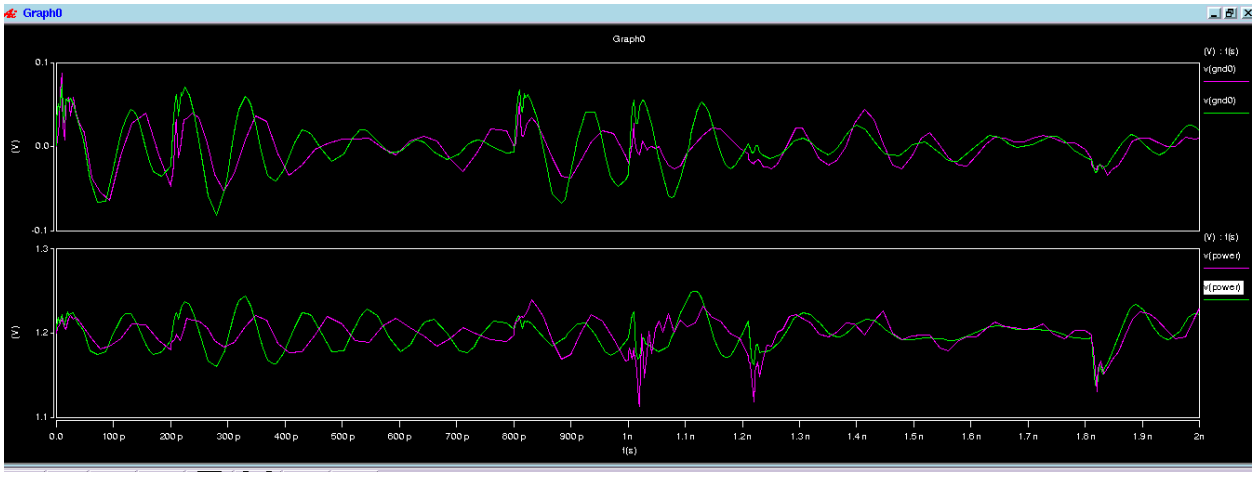

Figure 15 - Revised Baseline HSpice Simulation (Purple), 1st Iteration of Multi-Phase Simulation (Green)
NOTE: coupling capacitance was not used at this point

Getting the exact capacitive value of the circuit would entail making a layout of each circuit and using this tool to estimate the exact capacitance. It would also entail the need to learn new software to understand 65nm modeling rules and techniques, not to mention that different versions of the same circuit will have different capacitance values. The time needed to for that effort was not figured in with the allotted time for this project, so, by running several simulations starting with a large capacitance and adjusting the value until there was a reasonable approximation for a determined relative capacitive value for both the internal power and ground rails. After several simulations, a 100pF coupling capacitor for both the power and ground rails was chosen. The output response is shown below in Figure 16. This capacitance was applied to the Multi-Phase package model as depicted in Figure 1, Phase 2.

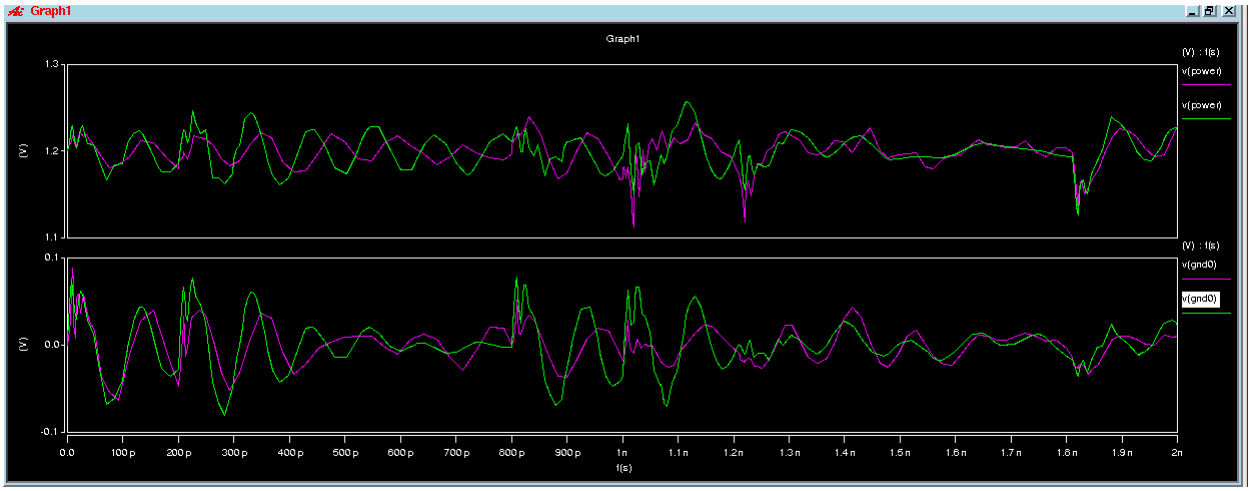

Figure 16 - Baseline HSpice Simulation (Purple), 1st Iteration of Multi-Phase Simulation (Green)
NOTE: using coupling capacitors of 100pF each

The waveform comparison between the baseline simulation and the Multi-Phase simulation are noticeably different even though there are closer similarities. Information was found on the website for HSIM^{plus} that might explain these variances stating the simulations contain nodal voltage information and use that information for the internal second-phase calculations [2]. Since the simulations are stopped and restarted with the collected output of each phase, there is lost information that cannot be transferred without significant alterations to the software. Another reason that could also contribute to the differing values is the replacement of a capacitive network (the die) with a singular capacitance on the power node and the ground node. This last reason could possibly have less of an impact if there was a simpler filtering scheme that has capacitive, resistive, and inductive elements.

Table 1 shows the multiple iterations of the 4-inverter circuit and times it took to run to completion. All of these simulations occurred in the CADE lab directly because remote logging resulted in simulations completing 3 to

4 times the duration than when simulated at the computer directly causing skewed results. Because of the possibility of multiple users on each of these computers from remote logging, the 'Real Time' and 'User Time' will be different values. The first iteration has slightly faster completion times than the original baseline simulation. This is to be expected because of two reasons: the loss of voltage information that the system deletes after we close the first simulation in order to begin anew, therefore, doesn't need to be calculated and the capacitive network that is replaced with a single capacitor and thereby narrows the amount of circuit calculations needed. During the Multi-Phase simulations, the difference between the first iteration and the second iteration is quite severe (see Figure 17), but as we perform further iterations, we can see the tenth iteration waveform matches the first iteration with considerable smoothing (see Figure 18). This smoothing is the waveform converging, but it is converging to a value that further away from the HSpice simulation values, not closer to the HSpice values as hoped for.

Table 1 – Simulation Times for Multiple Iterations of the Multi-Phase Approach Compared to Original Baseline HSpice Simulation

	Inverter (in seconds)		
	Real Time	**User Time**	**System Time**
Baseline	20.77	19.29	0.08
End of Iteration 1	16.32	15.21	0.09
End of Iteration 2	23.05	22.66	0.07
End of Iteration 3	21.46	21.06	0.12
End of Iteration 4	22.18	21.76	0.1
End of Iteration 5	24.66	23	0.11
End of Iteration 6	24.85	24.4	0.1
End of Iteration 7	25.9	24.37	0.1
End of Iteration 8	25.17	24.74	0.1
End of Iteration 9	27.14	25.68	0.1
End of Iteration 10	29	28.53	0.11

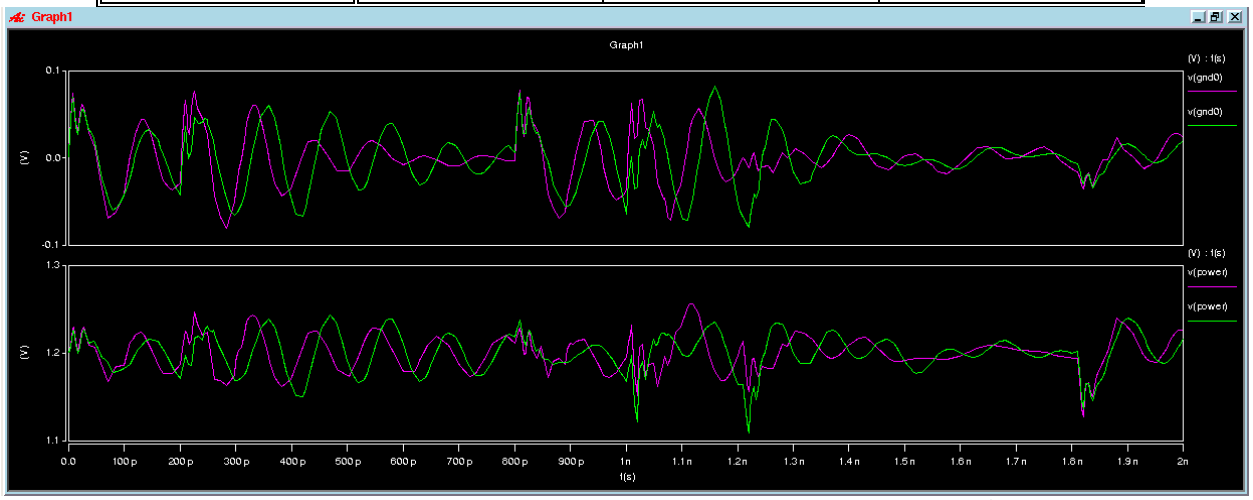

Figure 17 – 1st Iteration (Purple), 2nd Iteration (Green). NOTE: using coupling capacitors of 100pF each

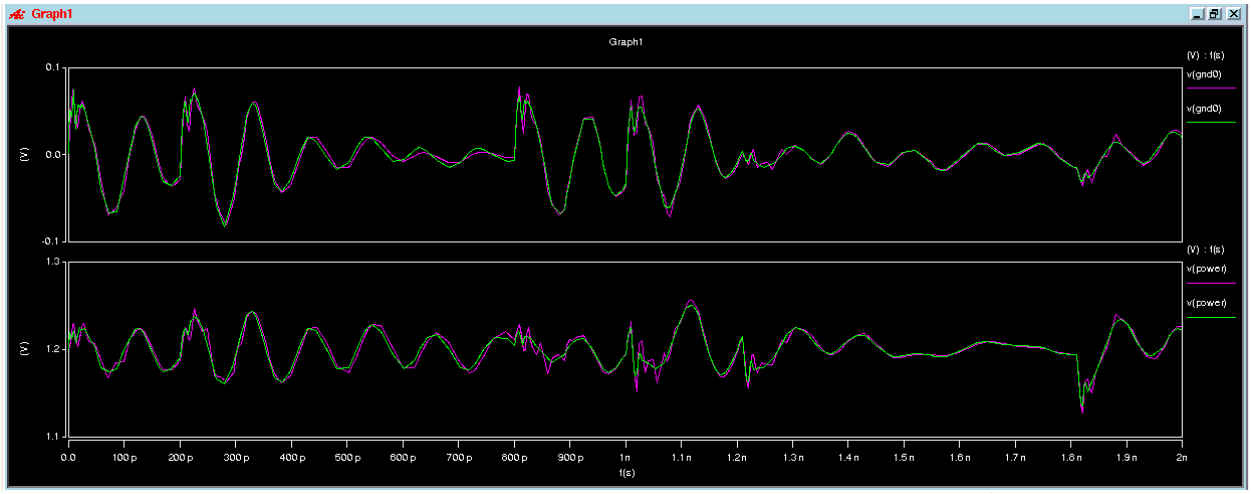

Figure 18 - 1st Iteration (Purple), 10th Iteration (Green). NOTE: using coupling capacitors of 100pF each

Below are some of the other circuit responses with the single capacitive value. We see that in the adder (see Figure 19) and multiplier (see Figure 20) circuits, the power rail responses are getting farther away when using a singular capacitive value. The 4-stage Fibonacci circuit (see Figure 21) began to be unstable; the voltage rail values increased with each Multi-Phase iteration until they came close enough to infinity to crash the simulation. The 8-stage and 16-stage Fibonacci circuits behaved similarly to the 4-stage Fibonacci circuit, which crashed around the 6th iteration. The 8-stage Fibonacci circuit crashed around the 4th iteration and the 16-stage Fibonacci circuit crashed after only 2 iterations. Because of this observation, there arose the need for the final modification to the second phase of the Multi-Phase circuit.

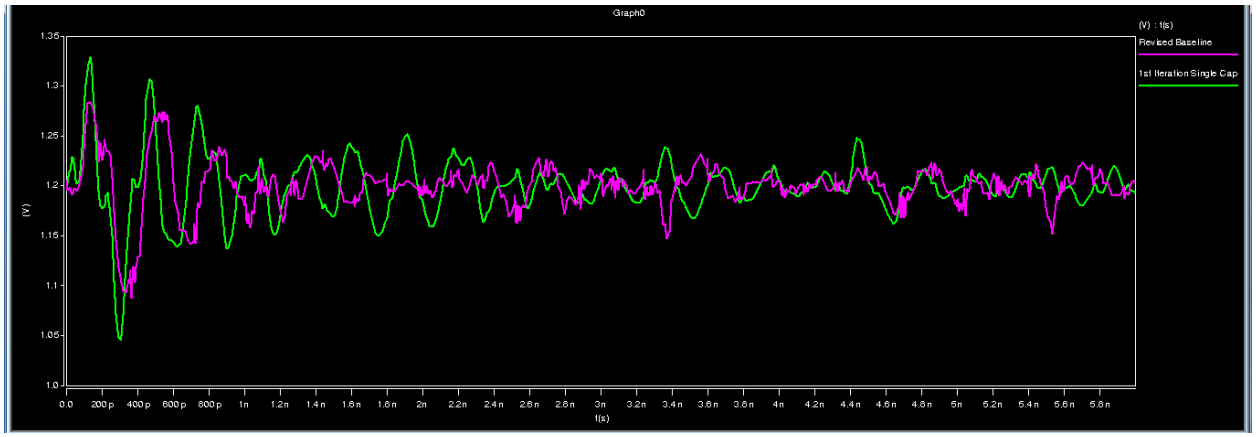

Figure 19 - 16-Bit Adder Baseline (Purple), 1st Iteration Multi-Phase (Green)

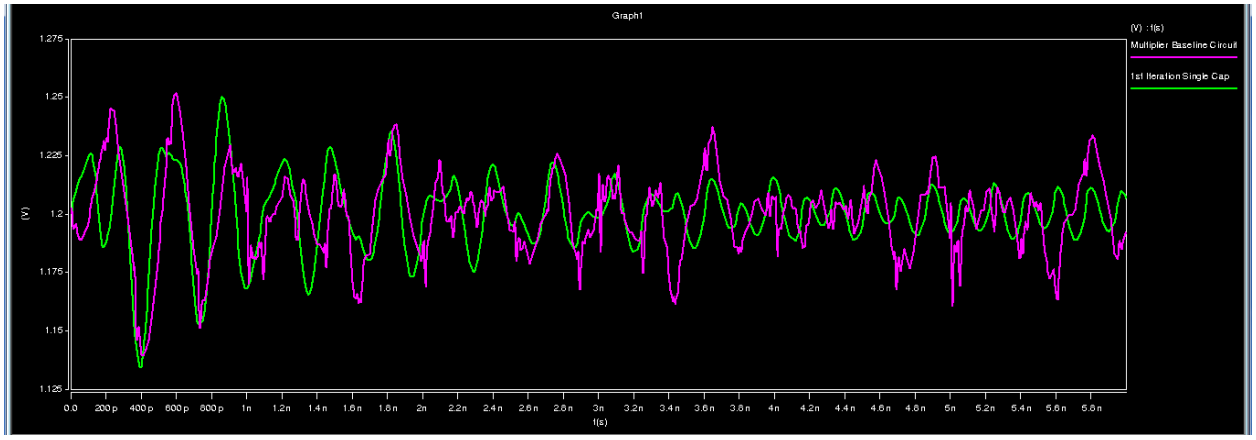

Figure 20 - 8-Bit Multiplier Baseline (Purple), 1st Iteration Multi-Phase (Green)

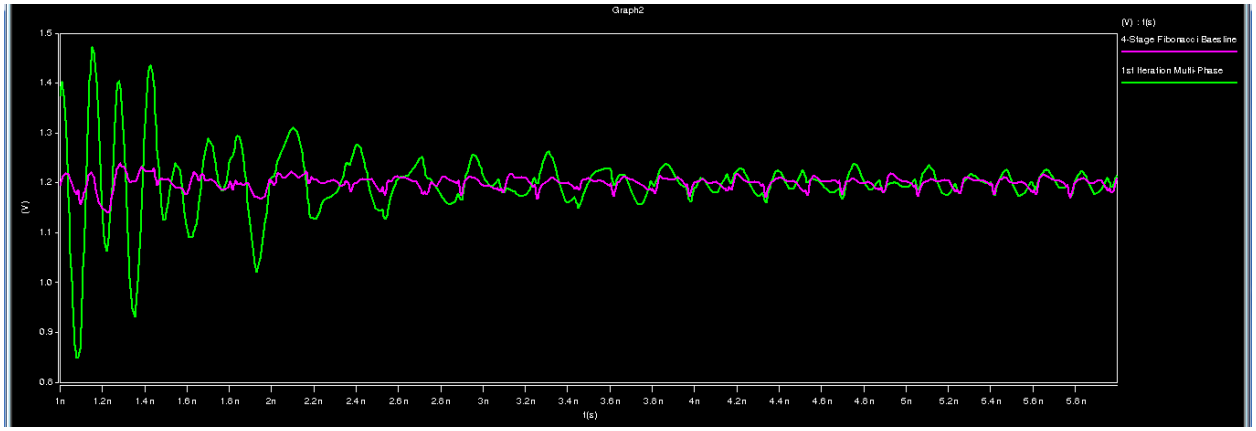

Figure 21 - 4-Stage Fibonacci Baseline (Purple), 1st Iteration Multi-Phase (Green)

Not only are we dropping a capacitive value by removing the die, but we are also removing resistive and inductive elements from the circuit, these values would keep the larger circuits from becoming unstable. There needed to be this resistive and capacitive element added back into the circuit as described in the methods section above. The circuit that was removed from the die was placed back into the circuit with 1 to 2 pF capacitor terminations (depending on the circuit) on all inputs and outputs. This would re-introduce the passive elements that were removed from the circuit without having to develop individual circuit filtering schemes. The output waveforms of all of the circuits are shown below in Figures 22 to Figure 27.

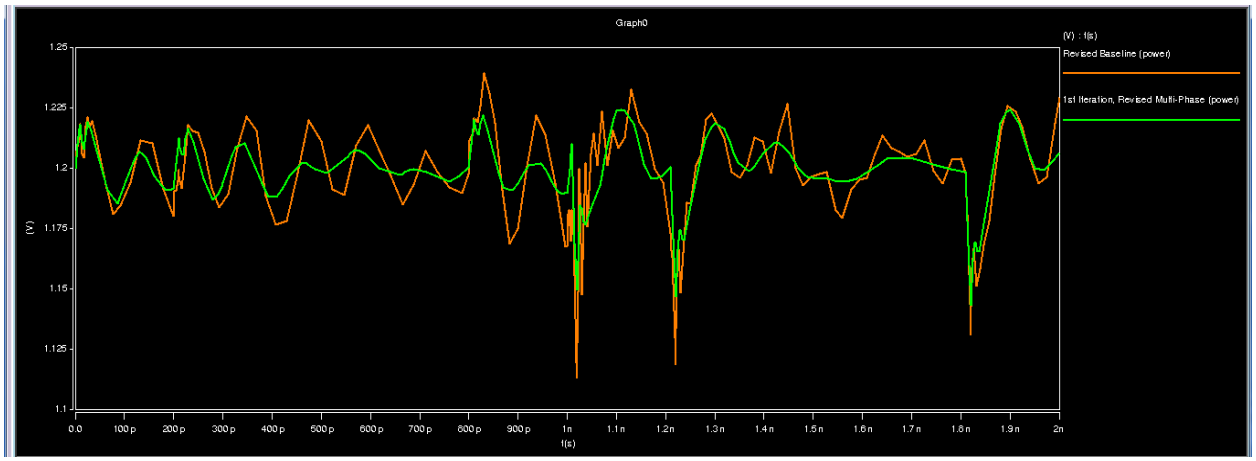

Figure 22 - 4-Inverter Revised Baseline (Orange), 1st Iteration of Terminated Circuit (Green)

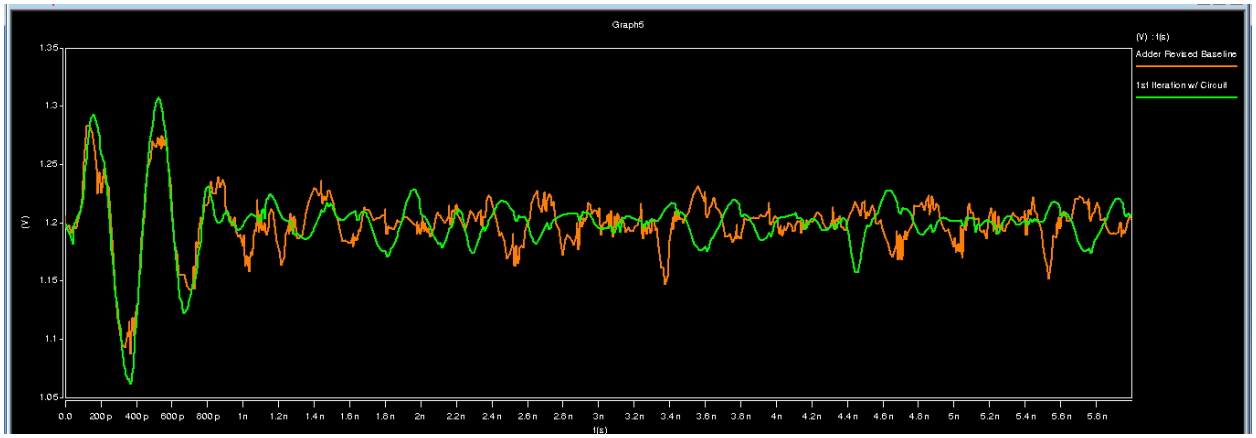

Figure 23 - 16-bit Adder Revised Baseline (Orange), 1st Iteration of Terminated Circuit (Green)

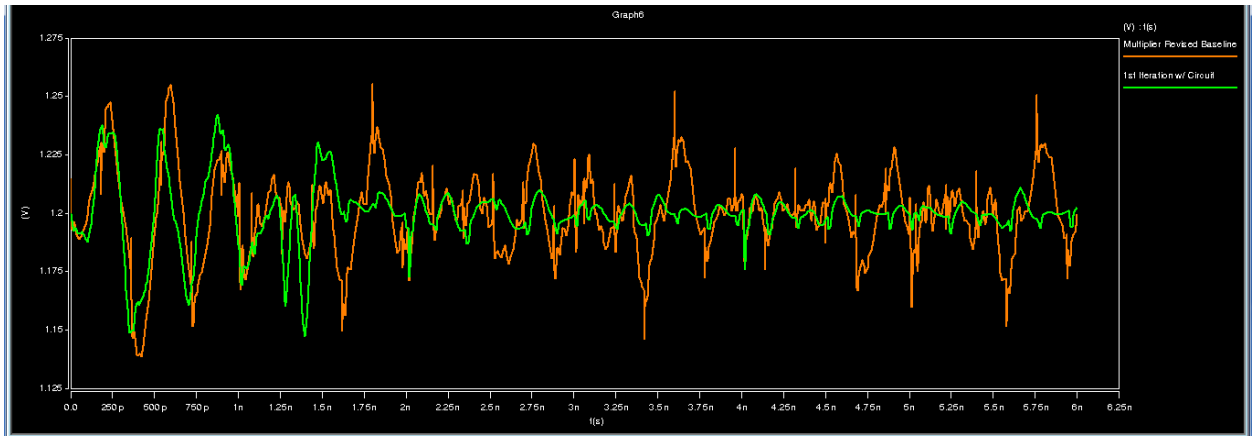

Figure 12 - 8-bit Multiplier Revised Baseline (Orange), 1st Iteration of Terminated Circuit (Green)

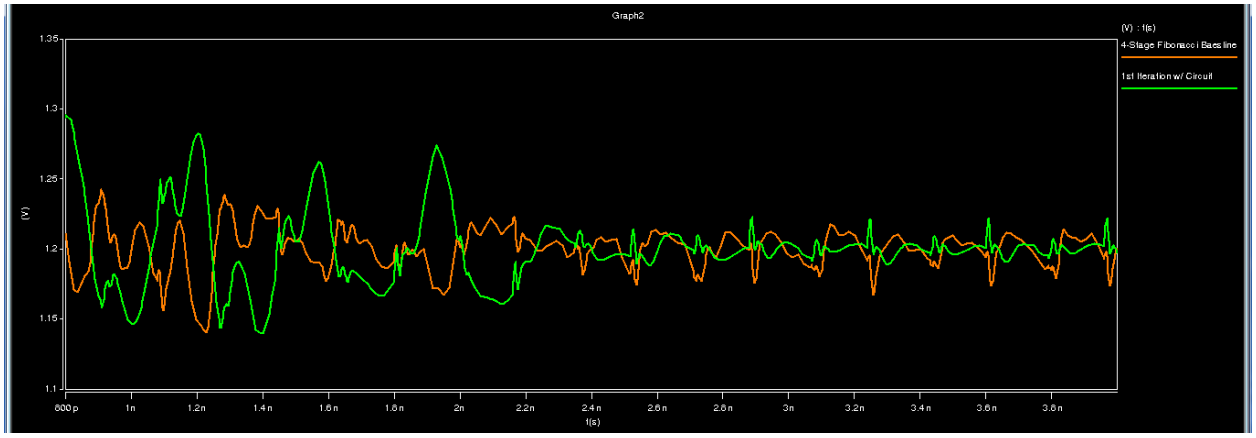

Figure 25 - 4-Stage Fibonacci Baseline (Orange), 1st Iteration of Terminated Circuit (Green)

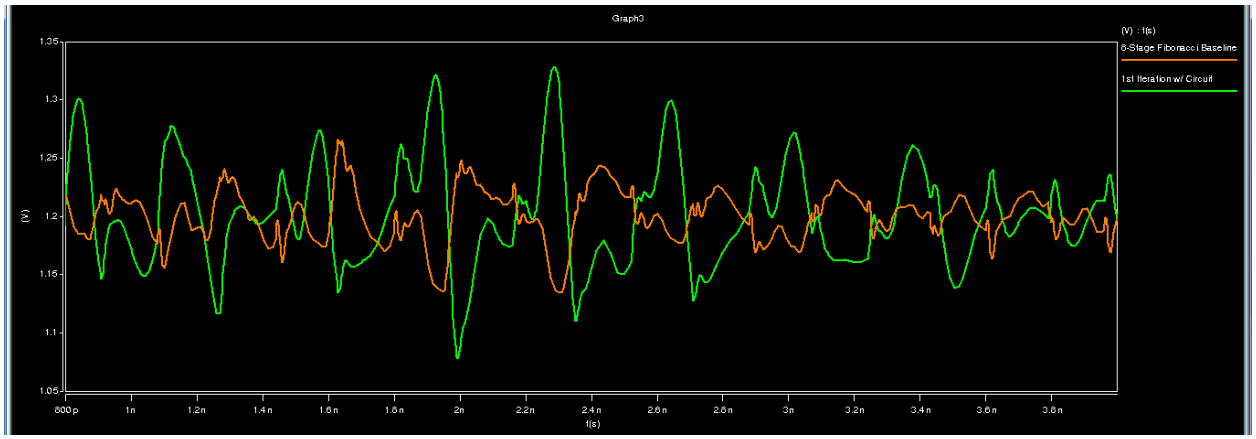

Figure 13 - 8-Stage Fibonacci Baseline (Orange), 1st Iteration of Terminated Circuit (Green)

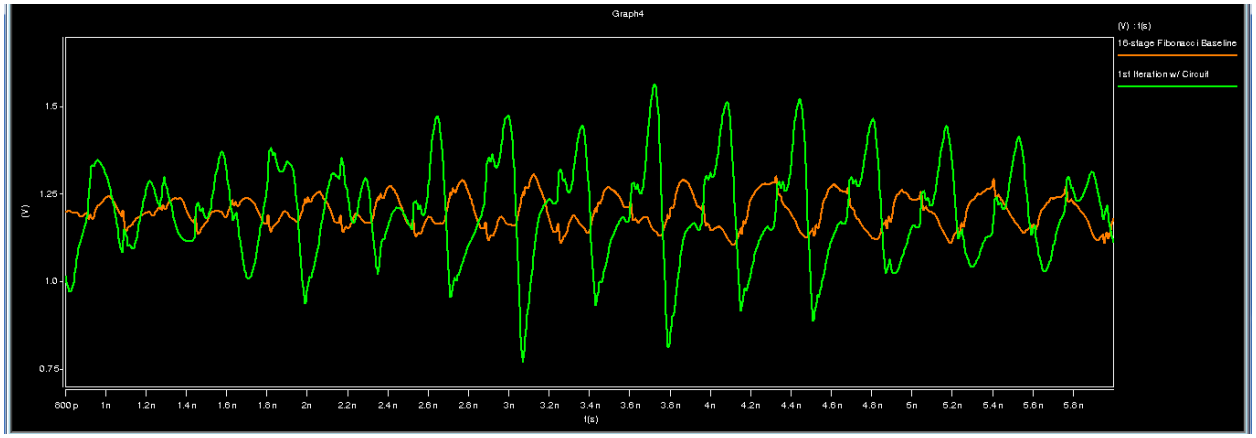

Figure 27 - 16-Stage Fibonacci Baseline (Orange), 1st Iteration of Terminated Circuit (Green)

Table 2 has all of the simulation information gathered from adding in the terminated circuits into the second phase of the Multi-Phase approach. Here longer simulation times are observed. This is due to the increased

calculations that are needed because of the capacitive, resistive, and inductive elements that have been added back into the second phase of the Multi-Phase simulations.

Table 2 - Simulation Times for Terminated Circuits in Second Phase of Multi-Phase Approach

	Inverter (in seconds)		
	REAL TIME	**USER TIME**	**SYSTEM TIME**
HSpice Baseline	20.77	19.29	0.08
Terminated Circuit 1	38.06	36.68	0.1
Terminated Circuit 2	49.35	47.12	0.09
Terminated Circuit 3	46.1	45.34	0.08
Terminated Circuit 4	49.76	45.36	0.11
Terminated Circuit 5	53.89	46.57	0.07
Terminated Circuit 6	47.23	46.37	0.06
Terminated Circuit 7	47.93	46.4	0.08
Terminated Circuit 8	47.93	46.4	0.08
Terminated Circuit 9	49.52	45.48	0.07
Terminated Circuit 10	46.01	45.07	0.05

	Adder (in seconds)		
	REAL TIME	**USER TIME**	**SYSTEM TIME**
HSpice Baseline	78.05	76.7	1.13
Terminated Circuit 1	153.2	145.57	0.44
Terminated Circuit 2	198.65	193.3	1.6
Terminated Circuit 3	221.96	218.34	1.83

	Multiplier (in seconds)		
	REAL TIME	**USER TIME**	**SYSTEM TIME**
HSpice Baseline	132.14	131.08	0.87
Terminated Circuit 1	166.88	160.81	0.89
Terminated Circuit 2	189.54	186.52	1.64
Terminated Circuit 3	196.1	193.39	1.36

	Fibinocci 4-stage (in seconds)		
	REAL TIME	**USER TIME**	**SYSTEM TIME**
HSpice Baseline	117.83	117.05	1.1
Terminated Circuit 1	222.62	209.28	1.8
Terminated Circuit 2	218.26	218.26	1.17
Terminated Circuit 3	240.19	236.9	1.35

	Fibinocci 8-stage (in seconds)		
	REAL TIME	**USER TIME**	**SYSTEM TIME**
HSpice Baseline	200.4	199.5	0.45
Terminated Circuit 1	344.65	342.28	1.48
Terminated Circuit 2	654.23	632.29	2.65

	Fibinocci 16-stage (in seconds)		
	REAL TIME	**USER TIME**	**SYSTEM TIME**
HSpice Baseline	321.16	314.21	1.2
Terminated Circuit 1	1142.47	1138.84	1.23
Terminated Circuit 2	2848.44	2839.49	6.22

Another intention of the Multi-Phase approach was to compare its voltage and ground rail values to values simulated on HSpice and HSIM^{plus} to see whether or not the power and ground rails converged to some value. Shown in Figure 28are comparisons of the HSpice baseline, the 1st iteration of the Multi-Phase approach, and the 10th iteration of the Multi-Phase approach. In Figure 29, we can see the comparisons between the 4-stage inverter HSpice baseline, HSIM^{plus} baseline, and 1st iteration of the Multi-Phase approach. Here is noticed the values of the power rails converged. However, the values that converged resemble that of HSIM^{plus}, instead of HSpice values as was hoped for.

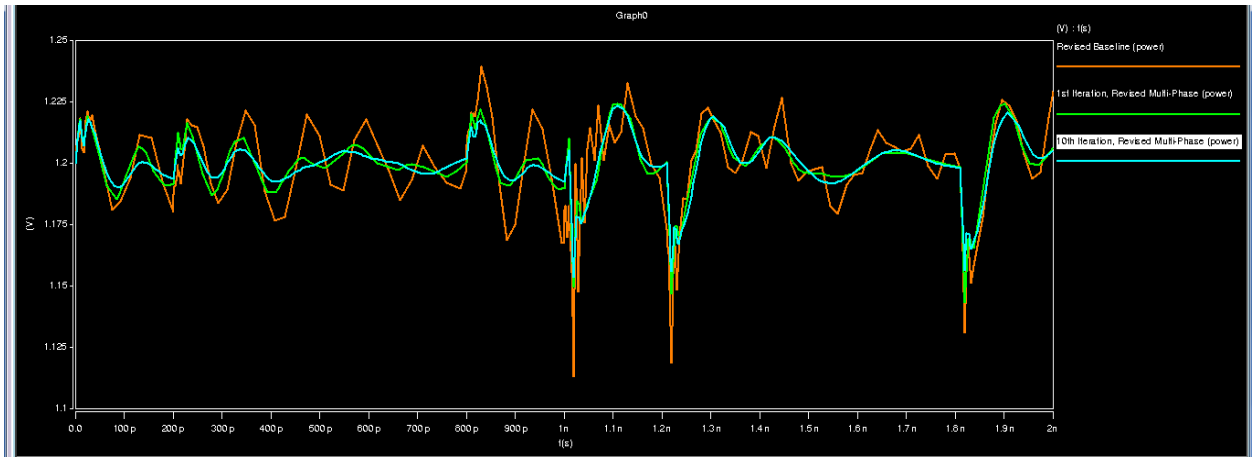

Figure 28 - 4-Inverter HSpice Baseline (Orange), 1st Iteration Multi-Phase (Green), 10th Iteration Multi-Phase (Blue)

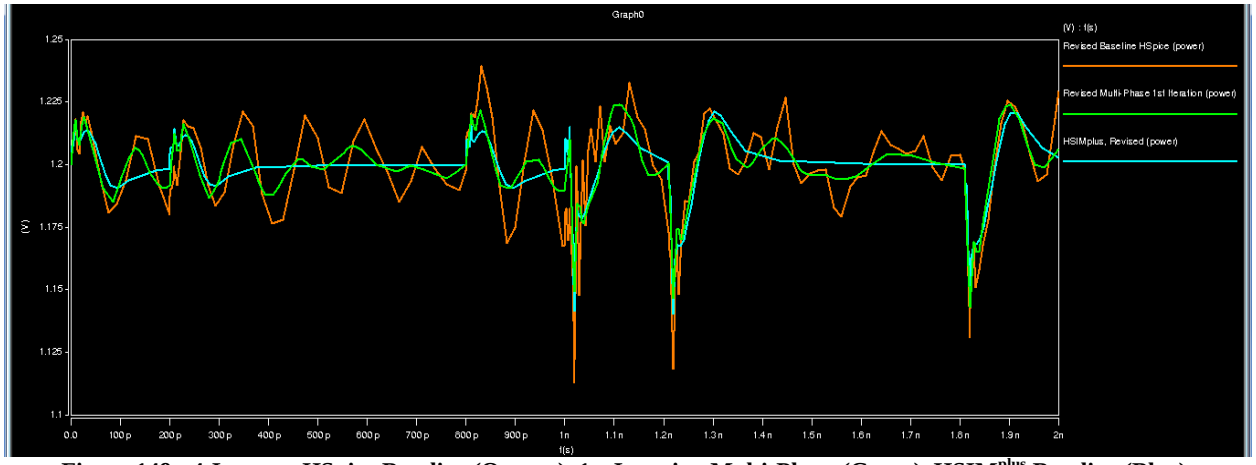

Figure 149 - 4-Inverter HSpice Baseline (Orange), 1st Iteration Multi-Phase (Green), HSIM^{plus} Baseline (Blue)

Finally, a new comparison with the revised baseline circuits were made between HSpice and HSIM^{plus} to see what the new values would be using the revised baseline circuits. The results shown in Table 3 were not predicted but they can be explained. HSIM^{plus} is used in industry because it is a faster simulator albeit with less accuracy. The simulations that are usually performed with HSIM^{plus} are much larger and much more complex compared to the circuits we are testing with this process. Table 3 shows that HSpice simulated faster than HSIM^{plus} in all cases for all precision levels on all circuits. HSIM^{plus} uses a set method for calculation that is labor intensive at the beginning but labor light for longer simulations, whereas HSpice simulation duration follows according to amount of transistors to be calculated almost linearly according to simulations as proved by the results from the team least year [5].

Table 3 - HSIM^{plus} Simulation Times Compared to HSpice

	4-INVERTER					
HSIMplus Precision	**Level 0**	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**HSpice**
MOS evaluations	18,176	18,208	18,208	18,208	21,632	
Time (in seconds)	20.696	20.684	20.706	20.766	43.958	19.29

	16-BIT ADDER					
HSIMplus Precision	**Level 0**	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**HSpice**
MOS evaluations	488,008	485,562	544,118	543,272	1,959,856	
Time (in seconds)	164.43	164.32	168.47	164.53	343.5	76.7

	8-BIT MULTIPLIER					
HSIMplus Precision	**Level 0**	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**HSpice**
MOS evaluations	7,447,602	7,450,026	7,526,926	7,461,290	10,113,416	
Time (in seconds)	298.03	294.91	303.61	294.08	621.24	131.08

	4-STAGE FIB					
HSIMplus Precision	**Level 0**	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**HSpice**
MOS evaluations	2,115,926	2,121,662	2,193,106	2,233,582	7,450,784	
Time (in seconds)	161.33	163.87	164.3	160.91	350.48	117.05

	8-STAGE FIB					
HSIMplus Precision	**Level 0**	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**HSpice**
MOS evaluations	5,801,828	5,794,150	5,926,943	6,006,732	20,997,664	
Time (in seconds)	227.73	226.36	230.58	227.69	495.74	199.5

	16-STAGE FIB					
HSIMplus Precision	**Level 0**	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**HSpice**
MOS evaluations	22,216,158	22,667,222	22,017,499	22,584,616	74,063,680	
Time (in seconds)	405.72	408.4	409.02	407.29	940.17	314.21

B. Voltage Controlled Resistor Function

The first current waveform that we attempted to reproduce using the VCR was from the 4-inverter circuit. Figure 30 shows the current that was drawn from the positive power rail of the inverter circuit and the current that was produced by the VCR current generating circuit. The VCR circuit was able to reproduce the current waveform from

the inverter circuit accurately. There was a maximum percentage error of 8.5% between the two waveforms, with an average percent error of only .15%. At this point it appeared that the VCR will definitely be able to replace the current source in the two-phase model. However, when more complex circuits are simulated, we begin to see a problem with the VCR.

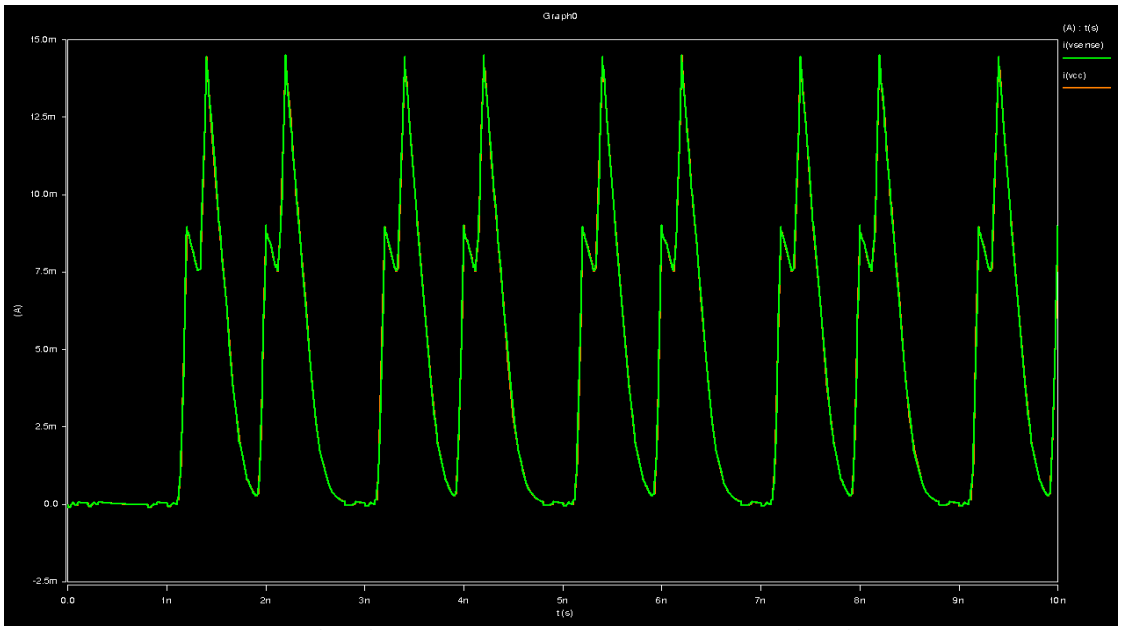

Figure 30 - Current Waveform from Inverter Circuit (Orange). Current Waveform from VCR Circuit (Green)

Figure 31 shows the current drawn by the 16-bit multiplier circuit from the positive power rail and the current that was produced by the VCR circuit.

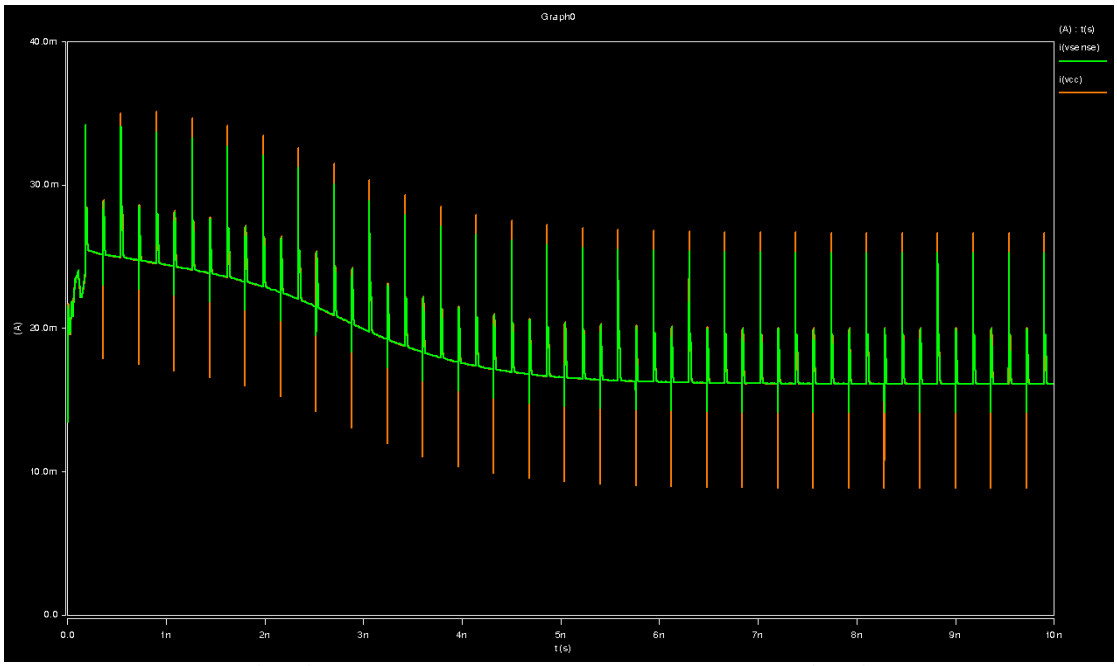

Figure 31 - Current Waveform from 16-bit Multiplier Circuit (Orange). Current Waveform from VCR Circuit (Green)

While the VCR circuit is able to match the multiplier current fairly closely there is a discernable difference between the waveforms. This difference is most apparent at the sharp spikes of current. It appears that the resistance used in the current generating circuit has caused a loss of some of the higher frequency components of the current and that is why so much error is occurring at the spikes in current. For the multiplier circuit the maximum percentage error in current was 71%, while the average percent error was just 0.18%. This large maximum error but small average error indicates that there are a small number of points with large error. These points of large error are located around the spikes in current. As even more complicated circuits are simulated the same trend is observed.

Figure 32 shows the current drawn by the Fibinocci-16 circuit from the positive power rail and the current generated by the VCR circuit. Again large errors are observed around the sharp spikes in current as a result of losing high frequency components of the current due to the resistance in the current generating circuit. For the Fibinocci-16 circuit the maximum percentage error was 285%, while the average error was 1.2%. As the simulated circuits get more and more complicated more error is introduced by the VCR. This indicated that these larger circuits cannot be modeled with just a single VCR.

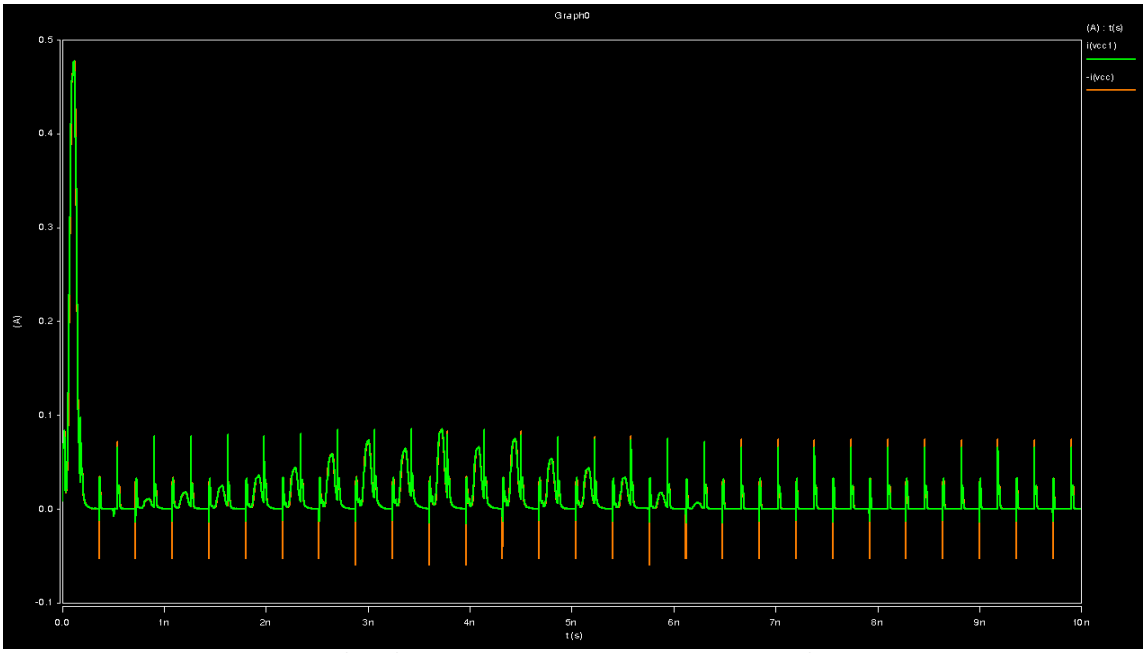

Figure 32 - Current Waveform from Fibinocci-16 Circuit (Orange). Current from VCR circuit (Green)

Something to consider is that in a two-phase analysis these complex circuits would be broken down into smaller parts and the current draw of each of the parts would be modeled by a separate current source [1]. The currents from these small parts may not have these sharp changes in current. It may be that only when the currents from all the parts are added together that the total current drawn from the power supply has these sharp spikes. This would mean

that if these complex circuits were broken down into smaller parts and the current draw of the small parts was recreated with the VCR, the results may be a much more accurate reproduction of the current waveforms. To test this hypothesis, the 4-inverter circuit was revisited. This time, instead of modeling the total current draw of all four inverters with a single VCR, the current draw of each inverter was modeled with a separate VCR. Figure 33 shows the current drawn by a single inverter, as well as the total current drawn by all four inverters and the current generated by the VCR circuit. As predicted the current drawn by a single inverter is a simpler waveform than the total current drawn by all four inverters. Also as predicted the VCR was able to more accurately model the current drawn by each inverter, resulting in a more accurate reproduction of the total current waveform. In this test the maximum percentage error was 5.5%, while the average error was .14%. This implies that by breaking the larger, more complex circuits into small parts and modeling each of those parts with a VCR, it may be possible to decrease the loss of high frequency current components and improve the VCR's accuracy.

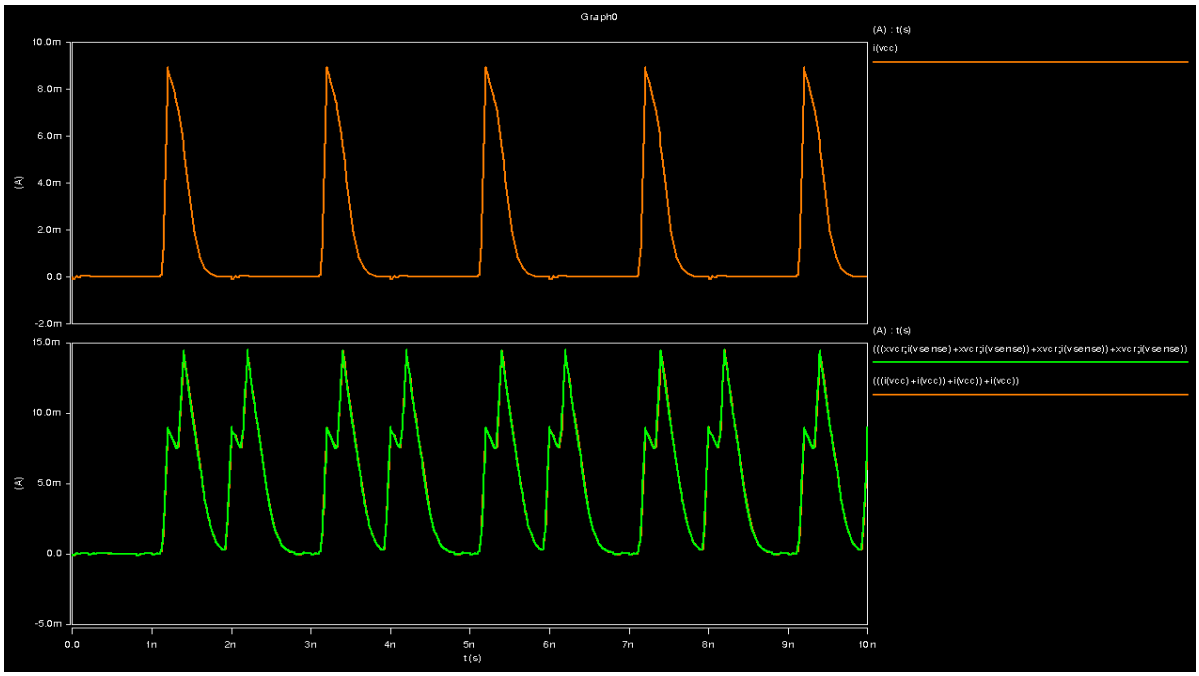

Figure 33 - Current drawn by a single inverter (Top). Total Current Drawn by Inverter Circuit (Bottom-Orange) Total Current Produced by VCRs (Bottom-Green).

In addition to potentially making simulations more accurate, using a VCR should also result in shorter simulation times than running a full HSpice simulation. To test this, the currents of all the test circuits were generated in three different ways: using the circuits themselves to generate the currents, using a VCR, and using a current source. These simulations were run three times each and the average times are shown in Table 4. From Table 4, as expected the VCR is much faster at producing currents than running a full simulation on a circuit. The VCR's simulation

time remains relatively constant regardless of circuit complexity, while the circuit simulation times increase greatly with circuit complexity. However, even though the VCR is faster than a full circuit simulation at generating currents, using a current source is slightly faster than the VCR.

Table 4 - Simulation Times

Circuit Simulated	Circuit		VCR		Current Source	
	CPU Time	Total Time	CPU Time	Total Time	CPU Time	Total Time
4-Inverter	.76 s	1.08 s	.07 s	.273 s	.07 s	.256 s
16-bit Adder	7.97 s	8.31 s	.08 s	.347 s	.08 s	.237 s
16-Bit Multiplier	27.8 s	28.9 s	.137 s	.44 s	.08 s	.327 s
Fibinocci-4	40.64 s	41.69 s	.107 s	.353 s	.077 s	.293 s
Fibinocci-8	91.6 s	95.46 s	.1 s	.363 s	.08 s	.305 s
Fibinocci-16	229.5 s	231.7 s	.12 s	.393 s	.08 s	.313 s

C. Voltage Controlled Resistor Implementation

For all of the VCR simulations, it was the VCC voltage results of the simulations that were the focus of analysis. After setting up the first configuration of the VCR circuit, a sensitivity test to varying resistance and capacitance was done. In the next two figures, the VCC voltages change as the resistor and capacitor sizes change. In Figure 34, it shows how the changing resistance affects the size of the amplitudes of the power voltage. The three different resistor sizes used were: 100 Ω, 1 kΩ, and 4 kΩ. In Figure 35, it shows how the changing capacitance affects the phase and amplitudes of the voltage spikes are some points. The three different capacitor sizes used were: 1 fF, 100 pF, and 1 mF. The results for 1 fF and 1 mF are pretty much the same, which is odd because the capacitances differ so much in value. The circuit is shown to be sensitive to the size of the capacitance.

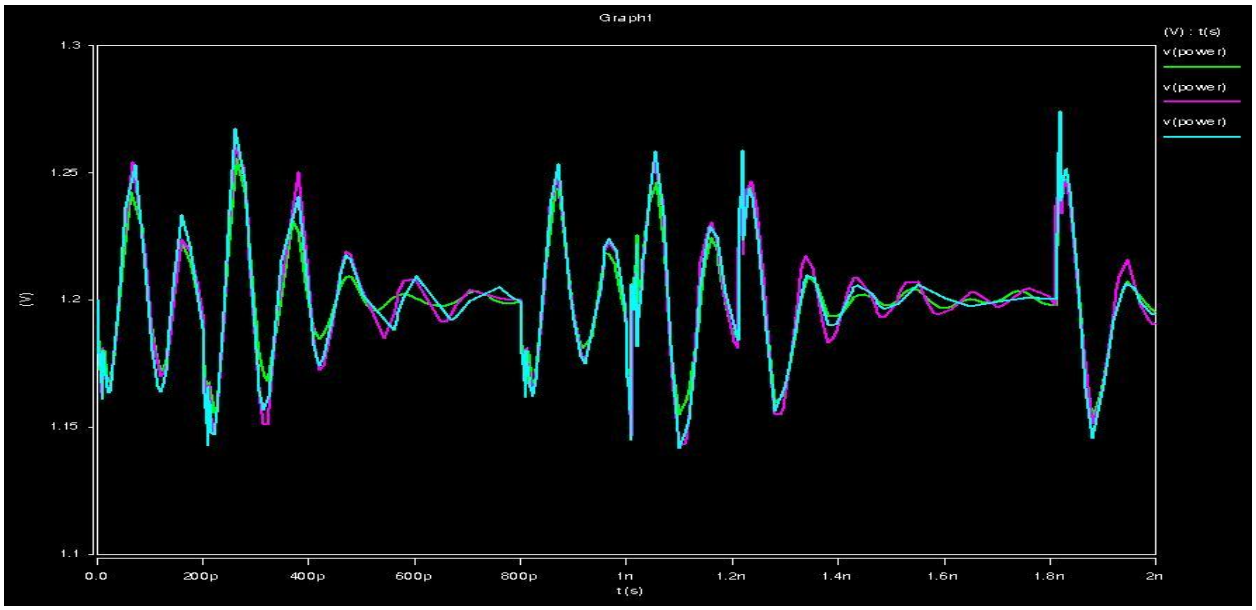

Figure 34 - Sensitivity of changing resistance 100 Ω (orange), 1 kΩ (blue), and 4 kΩ (purple)

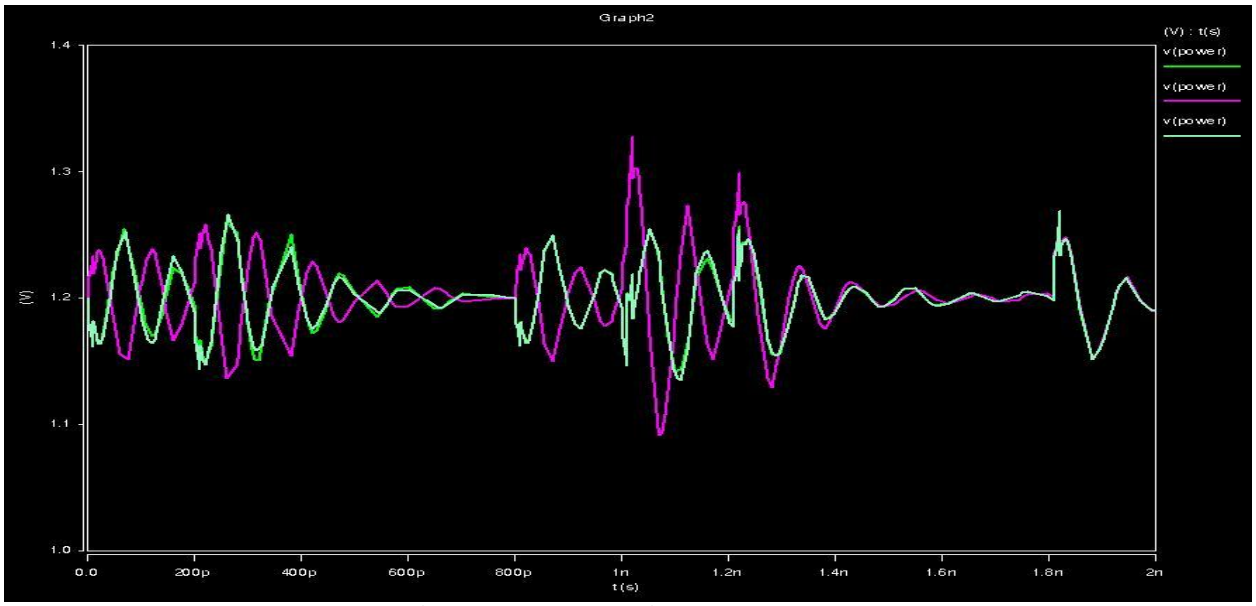

Figure 35 - Sensitivity of changing capacitance 1 fF (green), 100 pF (purple), and 1 mF (blue)

As mentioned earlier, these results didn't match up well with their respective baseline simulations so modifications had to be made in order for better consistency. As described, for each circuit there had to be modifications to the VCR circuit each time for the voltages to match up each time. But even after the modification, there were still messy power voltage signals and the single capacitor value was not enough to match the circuits' natural capacitance. In Figure 36 shows how the revised VCR circuit with the modifications results compares with HSpice baseline simulations.

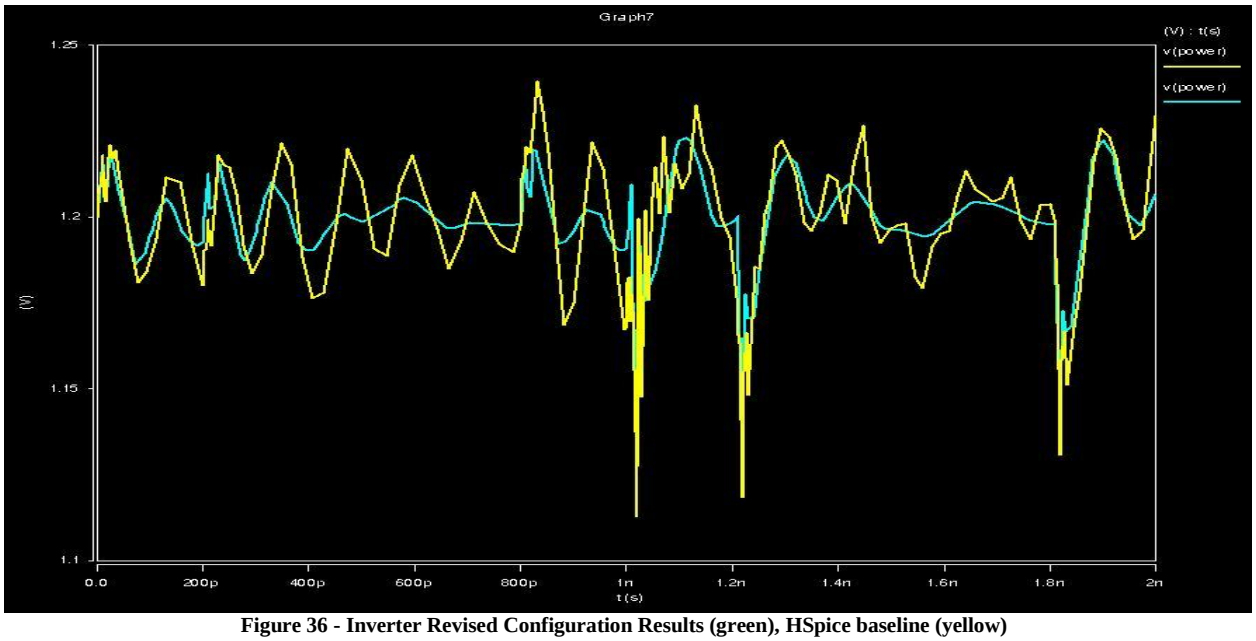

Figure 36 - Inverter Revised Configuration Results (green), HSpice baseline (yellow)

In Figure 36, the revised configuration and the HSpice results are a lot closer and in phase at most points. The VCC voltage was a lot cleaner when comparing with the same voltage for the initial configuration. Since the various modifications made the VCR configuration impractical, a single configuration would need to be found for all the circuits to use. With this new configuration the results were also more consistent with the baseline simulation. Below, Figures 37 and 38 show some of the results of the new practical configuration.

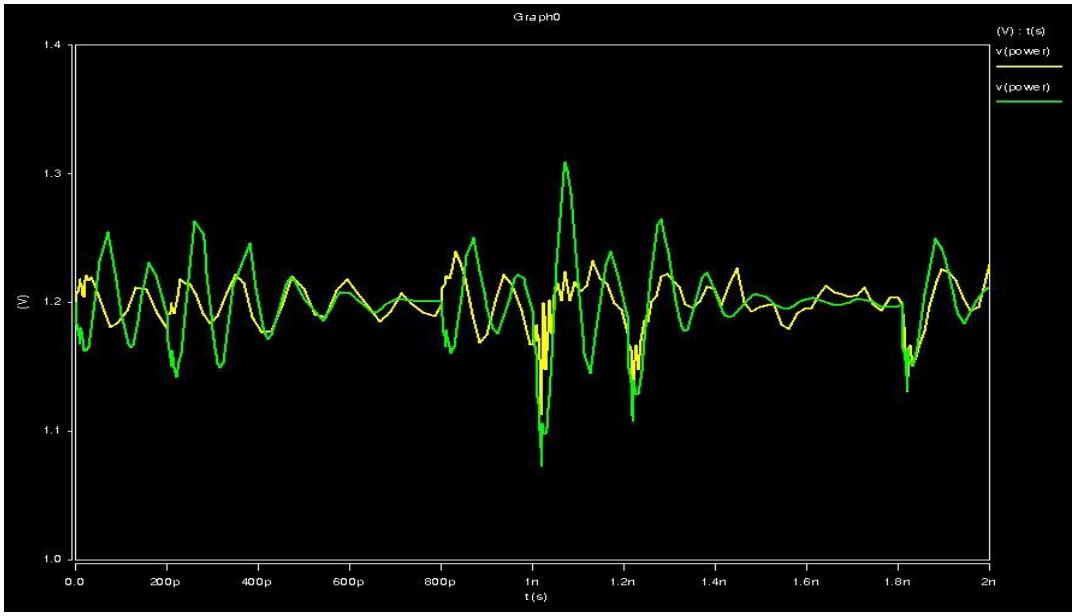

Figure 157 - Inverter New Configuration Results (green), HSpice baseline (yellow)

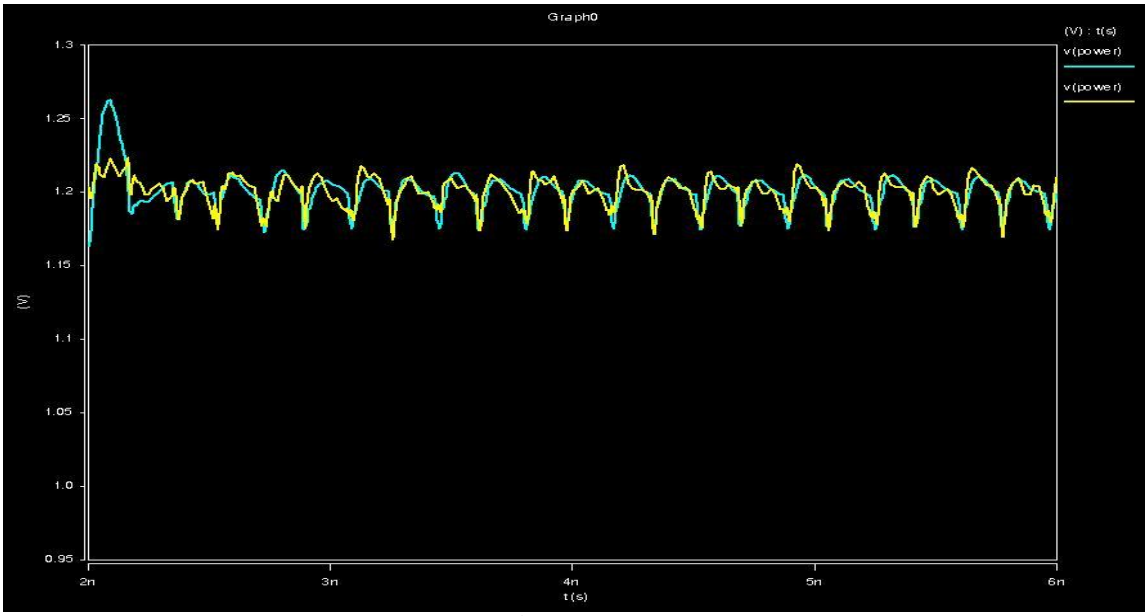

Figure 38 - 4-Stage Fibonacci New Configuration Results (green), HSpice baseline (yellow)

In these results there is more consistency with the HSPICE baseline simulations. The 4-Stage Fibonacci results are more in line with the baseline in Figure 38. The results for the 8-Stage and 16-Stage Fibonacci circuits are similar in that their results matched very well with the baseline simulation.

Even though the results were pretty close to the baseline simulations, the runtime of the simulations is another factor that must be taken into consideration. A simulation could be accurate but may take three times longer than the baseline simulation had taken to complete. Below in Table 5 are the runtimes of the HSpice baseline simulations and the runtimes of the new revised configuration of the VCR circuit.

Table 5 - Simulation Runtimes

Revised Two-Phase

	Real	User	Sys
Inverter	21.69	20.58	0.1
Adder	110.2	109.14	0.7
Fib 4	135.9	135.9	0.44
Fib 8	298.33	300.29	0.73
Fib 16	549.17	548.17	0.63
Multi	149.53	148.17	0.83

HSpice Simulation Package + Die

	Real	User	Sys
Inverter	20.77	19.29	0.08
Adder	78.05	76.7	1.13
Fib 4	117.83	117.05	1.1
Fib 8	200.4	199.5	0.45
Fib 16	321.16	314.21	1.2
Multi	132.14	131.08	0.87

The simulation times for the HSpice baseline are still shorter than the two-phase simulations. The simulation runtimes of the revised two-phase were a little longer but not very accurate.

After conducting all the simulations with the alternate two-phase VCR method, it seems that when compared to the baseline simulations, it didn't compare well. At first, the initial simulation runtimes with the baseline were

shorter but the accuracy was not there. So to improve the accuracy of the alternate two-phase VCR method a revised configuration of the VCR circuit was designed. Even though this configuration would prove to be more accurate than the previous configuration the runtimes of the simulations were longer than the baseline simulations. A problem encountered with the first configuration of the VCR circuit was that each circuit simulation required modifications that made the VCR circuits not practical not being universal from circuit to circuit.

The switching of the VCR polarities was done so that the voltage pulls emulate the baseline simulations. The creation of this problem came from how the current translation equation would affect the control voltage. Since the current is small and the resistor is large, it would result in the control voltage having some negative values and these negatives voltage affected how the VCR would operate. The currents from each circuit were unique and a single resistor to fix this problem was not realistic. A single configuration was found, however it did not help improve the runtime issue. There were still inconsistencies found in the Inverter results despite the fact that the revised configuration worked better for the rest of the circuits.

V. Future Work

Not everything that we had wished to work on was completed. One idea that we considered was using the VCR model and putting it through the multiphase analysis. Another aspect we did not get time to get to was replacing each individual transistor in each circuit with a VCR and analyzing the effects of that alteration. The last idea that was not looked into was, instead of just using HSpice in all our simulations, we would have also used HSIM^{plus} and analyzed the differences in the results between the two different programs. These were some of the ideas that did not get realized and we believe could be explored in a future project.

VI. Societal/Ethical Effects

The effect that this project has on society is that it will add to the base of knowledge that is available to people who are responsible for the validation and design of ICs. The hope is that from the experimentation performed here better methods for SPICE simulations can be created to assist in the creation of better electronics for the whole spectrum of applications. For the broad base of society, life simplifying/enhancing devices could be assisted in development by the work done in this project. These results could be used in any application where SPICE simulation is necessary, from Military/Defense applications to simple consumer electronics, and anywhere that micro-electronics might find their way in the future.

VII. Conclusions

The Multi-Phase approach was, at first, thought to be an easy solution to a complex problem. This turned out to be a false assumption. There were many simplifications that needed to take place in order to get to a baseline circuit that would compare well to a circuit that was divided into two pieces. A current source is not a simple drop-in replacement for an entire capacitive, resistive and inductive network. There may be simpler schemes of filtering that would allow us to maintain simplicity for calculations, but would increase the difficulty by trying to find those filtering schemes which would not be universal among all circuits. Simulation times for single capacitances ran faster through the first iteration, but became unstable with larger circuitry. Terminated circuits had more accuracy by allowing the capacitive, resistive and inductive network to passively interact with the simulations but did not create the level of accuracy sought for. The simulation times also increased dramatically with the terminated circuits. Not only did the simulation times increase, but with several iterations, the values did not converge to HSpice values, but to HSIM^{plus} values. The Multi-Phase approach does not seem to be a valid direction to go for either accuracy or a decrease in simulation time.

The VCR is able to accurately reproduce currents for very simple circuits. However, for larger more complex circuits high frequency components of the current waveforms are lost, resulting in large errors. This loss of high frequency components is attributed to the resistance of the VCR. Experimentation showed that it may be possible to recover some of the lost high frequency current components and improve the accuracy of the VCR by breaking large, complex circuits down into smaller parts and modeling each part with a VCR.

The alternate Two-Phase VCR approach turned out to be not as accurate and as fast as the baseline simulations. The experimentation of different configurations of the VCRs effected accuracy. Modifications were made to the initial configuration to get the best results. The various modifications made the VCR impractical even though accuracy was improved. Despite these changes, the simulation runtimes were longer than the baseline simulations. Looking at the tradeoffs of this approach, both accuracy and runtimes were lacking comparing to the baseline. The Two-Phase VCR approach did not met expectations.

VIII. Acknowledgments

The 2010-2011 Micron Clinic Team would like to thank the project sponsor Micron Technology, without whom the experimentation performed would not have been conducted, with a special thanks to our sponsor contact/advisor Dr. Tim Hollis. We would also like to acknowledge the advisor for this project, Dr. Ken Stevens, whose help and guidance has been invaluable.

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