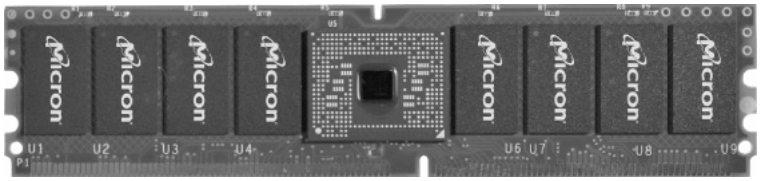
DRAM System
Signalling, Timing, Organization



Reference: "Memory Systems: Cache, DRAM, Disk

Bruce Jacob, Spencer Ng, & David Wang

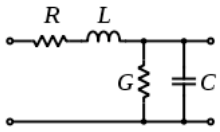
Today's material & any uncredited diagram came from chapters 9 & 10

Signal Integrity

- **Increasingly limiting in shrinking processes**
  - **gets even worse**
    - » **as speeds increase**
    - » **as trace length increases**
- **Multi-drop wires are a problem**
  - **very difficult to achieve perfect transmission line behavior in practice**
    - » **impedance changes with**
      - **temperature**
      - **manufacturing variability**
      - **L & C effects of the neighborhood**
      - **signal reflections**
  - **result is signal distortion**
    - » **made worse by noise**
      - **also a neighborhood problem**
- **DRAM systems**
  - **traces are long, and broadcast is the norm**
    - » **intra- and inter-device**

Transmission Line Behavior

- **Telegraphers equations**
  - **basically a simplified case of Maxwell's equations**
  - **lots of PDE's but key is lumped transmission line**
    - » **typical view is R & G are small - e.g. lossless line**
    - » **position x and time t and hence wave velocity v**



$$\frac{\partial}{\partial x}V(x,t) = -L\frac{\partial}{\partial t}I(x,t)$$

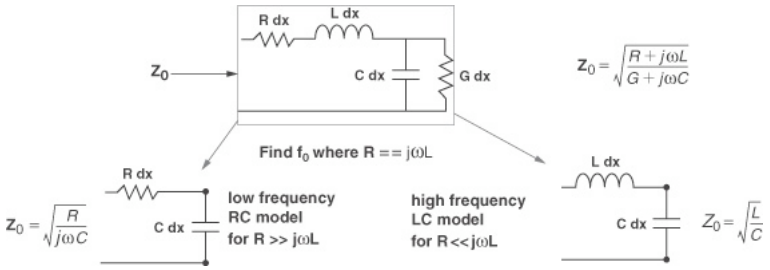
$$\frac{\partial}{\partial x}I(x,t) = -C\frac{\partial}{\partial t}V(x,t)$$

$$v = \frac{1}{\sqrt{LC}}$$

- » **key is that the phase shift of a propagating signal varies with its frequency**
  - **lots of frequency components in real signals**
  - **signal received is not the same as the signal sent**

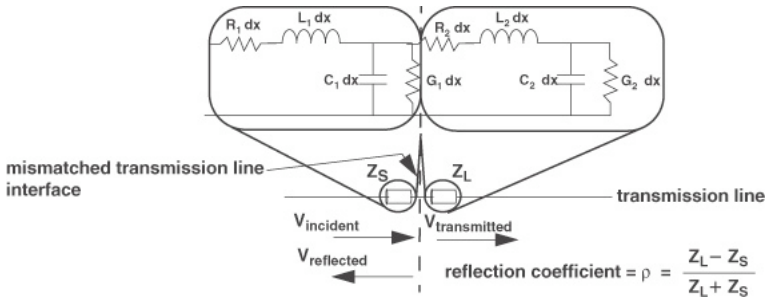
Two Signalling Regimes

- **Depends on the frequency**
  - **we try to stay in the RC world**
    - » **high frequency components enter due to reflections**

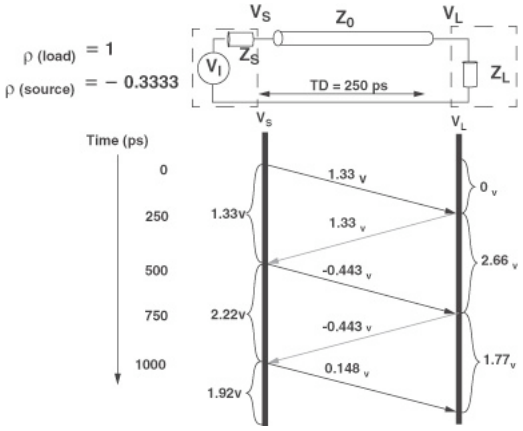


Reflection

- **Due to mismatched transmission line segments**



Non-Terminated Reflection Ladder



Assume

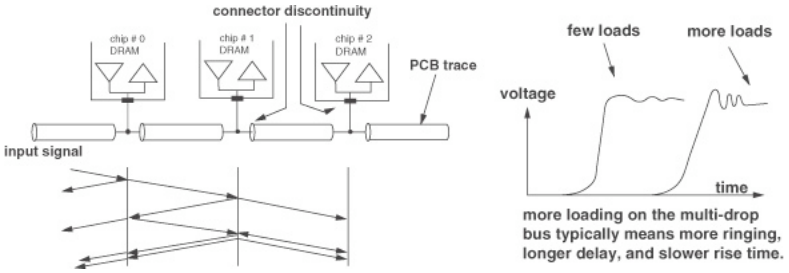
$Z_0 = 100\ \Omega$
$Z_S = 50\ \Omega$
$Z_L = \text{inf}$
$V_I = 2\ V$

$$V_S(\text{initial}) = V_I \frac{Z_0}{Z_s + Z_0}$$

$$= 1.33\ V$$

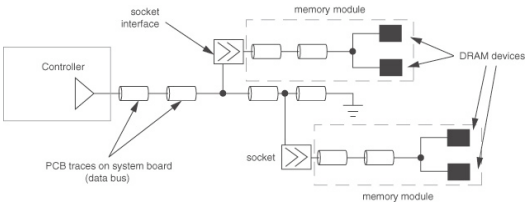
Multi-Drop Bus Complications

- **Result**
  - **as speeds increase**
    - » **#DIMMs per channel decrease**
    - » **delay added by slow rise time and let ringing settle**
      - **hmm - faster means more delay - huh?**
  - **socketed DIMM connector adds another discontinuity**
    - » **socket - PCB trace - connector - DIMM trace to DRAM die**



Other Complications

- **Skew**



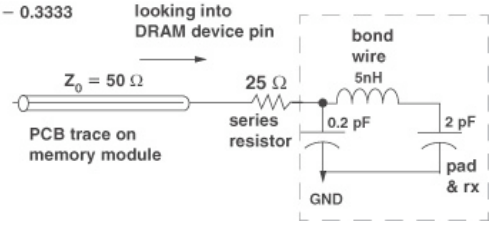
- **Jitter**
  - **small fluctuations in signal propagation velocity due to**
    - » **termperature, supply voltage, etc**
- **Inter-Symbol-Interference (ISI)**
  - **L & C induced cross-talk**
- **Bottom line**
  - **lots of practical barriers to increasing signal speed**

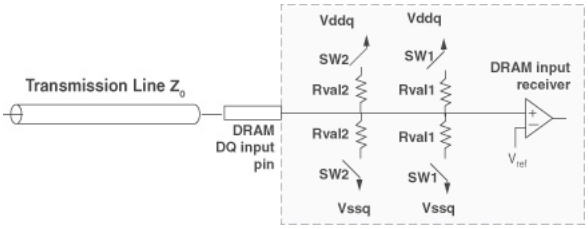
Termination

- **Key to minimizing reflections**
  - **but DRAM needs to be cheap**
    - » **cheap SOJ and TSOP packages**
      - **large pin C & L's - mismatched to trace impedance**
      - **OK for low freq - < 200 MHz**
  - **faster requires smaller pins ==> BGA (DDR) & FBGA (DDR2/3)**
- **Another termination issue**
  - **impedance inside vs. outside the package need to be isolated**
    - » **series termination (DDR)**
      - **damps internal DRAM component reflection effects on the DIMM trace**
    - » **programmable on die parallel termination (DDR2)**
      - **higher speeds ==> tighter reflection constraints**
      - **configuration register controls termination resistor switches**
      - **removes need to time for worst case configurations (max DIMMs)**

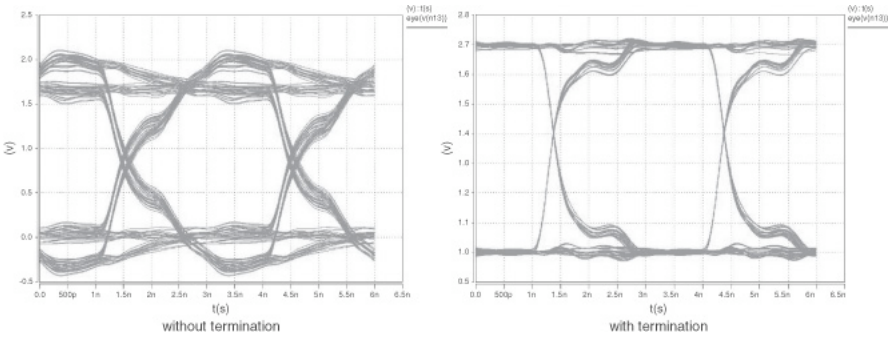
DDR Termination

$$\rho = \frac{Z_1 - 25 - Z_0}{Z_1 + 25 + Z_0} = -0.3333$$





Termination: Eye Doctor

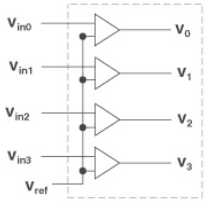


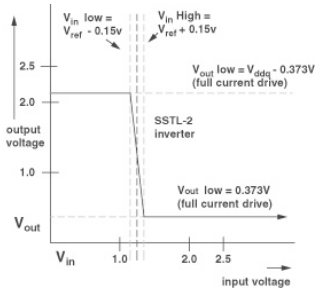
Voltage Issues

- **Low voltage swing**
  - **saves power and potentially improves speed**
  - **BUT: reduced noise immunity**
    - » **so do differential signalling**
    - » **problem - DRAM's have to be cheap**
      - **can't afford 2x data pins**
- **Vref**
  - **provide a common voltage reference used by all inputs**
    - » **adv: x+1 < 2x pins for interesting values of x**
    - » **disadv: lose the common mode rejection of differential**

DRAM Voltage Standards

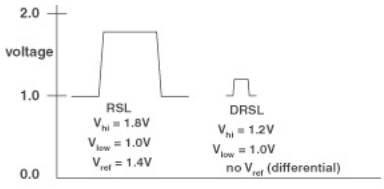
- **Series stub termination logic**
  - **SSTL_2 - used for 2.5v DDR parts**
  - **SSTL-18 - used for 1.8v DDR2 parts**
- **Similar idea just different standards**
  - **for SSTL_2, Vref = 1.25v**



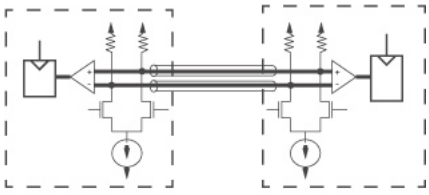


Rambus Versions

- **RSL - Direct RDRAM parts**
  - **Vref based but with lower swing**
- **DRSL - full differential, bidirectional, point to point**
  - **signaling interface must be isolated from core (mats)**
  - **fast but costly due to additional non-mat interface circuitry**



RSL and DRSL signaling levels



XDR signaling System (DRSL)

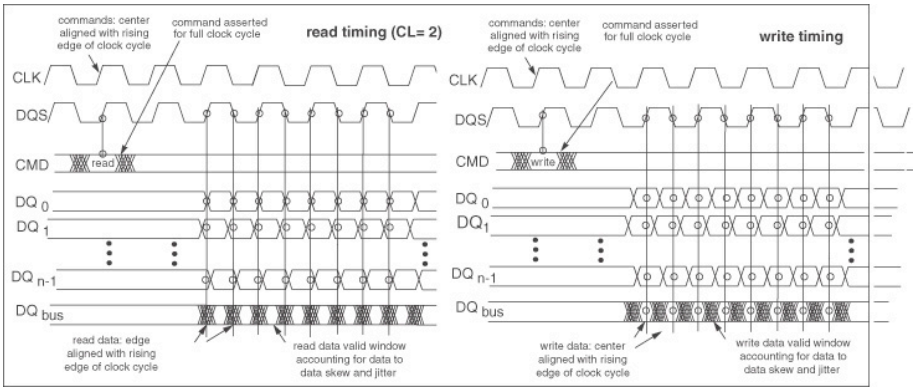
Timing

- Modern DRAM is synchronous
  - clock also a victim of
    - » skew, jitter, signal integrity
    - » broadcast nature means big L & C components
  - 3 clocking regimes
    - » global clock
      - slow since timing margin accomodates worst case
    - » source synchronous clock forwarding
      - RDRAM and DDR
    - » phase or delay compensated clocking
      - PLL or DLL synchronization in newest parts
        - DDR (DLL), XDR (PLL)
- Memory contoller gets more complex
  - responsible for timing and command sequence control
    - » needs to stay in the center of the eye

Control Addr vs. Data Bus

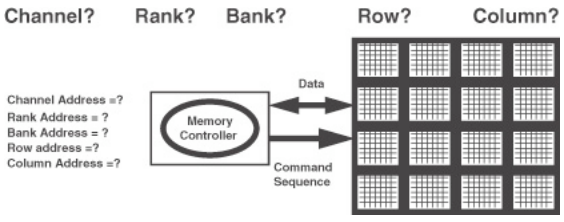
- Control and Address information is broadcast
  - higher bus load means slower
- Data is pseudo point-to-point
  - memory module knows if it's the addressee
    - » others go to Hi-Z connect to data bus
  - key to allowing the DDR scheme to work
  - DDR does complicate things however
    - » mem_ctl now needs to deal with 90 degree phase changes

Column Read & Write in DDRx

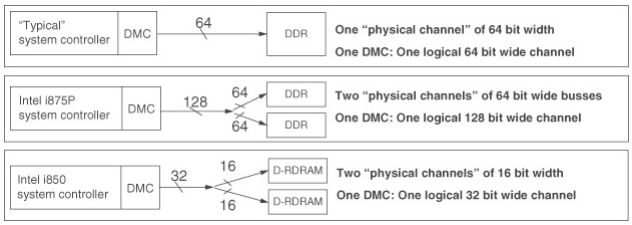


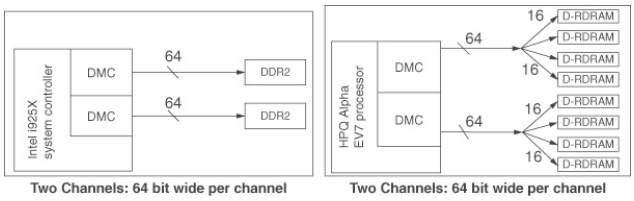
DRAM Organization

- **Remember**
  - **terminology varies with standard**
    - **» e.g. Rambus vs. JEDEC**
  - **and even within JEDEC by vendor to a lesser extent**
- **In general**



Vendor Channel Variation





Two Channels: 64 bit wide per channel

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DMC::= DRAM Memory Controller

DIMMs and DRAMs

DRAM chip type	DIMM Stick Type	Bus Clock Rate (MHz)	Memory Clock Rate (MHz)	Channel Bandwidth (GB/s)	non-ECC Channel Width	ECC Channel Width	Prefetch Buffer Width	Vdd	Read Latency Typical (bus cycles)	DIMM pins
DDR-200	PC-1600	100	100	1.6	64	72	2	2.5	2-3	184
DDR-266	PC-2100	133	133	2.133	64	72	2	2.5	2-3	184
DDR-333	PC-2700	167	167	2.667	64	72	2	2.5	2-3	184
DDR-400	PC3200	200	200	3.2	64	72	2	2.5	2-3	184
DDR2-400	PC2-3200	100	200	3.2	64	72	4	1.8	3-9	240
DDR2-533	PC2-4200	133	266	4.267	64	72	4	1.8	3-9	240
DDR2-667	PC2-5300	167	333	5.333	64	72	4	1.8	3-9	240
DDR2-800	PC2-6400	200	400	6.4	64	72	4	1.8	3-9	240
DDR3-800	PC3-6400	100	400	6.4	64	72	8	1.5	?	240
DDR3-1066	PC3-8500	133	533	8.53	64	72	8	1.5	?	240
DDR3-1333	PC3-10600	167	667	10.67	64	72	8	1.5	?	240
DDR3-1600	PC3-17000	200	1066	18.06	64	72	8	1.5	?	240