An FPGA Implementation of Whitted-style Ray Tracing Accelerator

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Abstract

This paper presents an FPGA implementation of a full whitted-style ray tracing accelerator. It achieves about 1.3M rays per second over realistic 3D scenes. The future implementation with ASIC is expected to achieve real-time performance.

Keywords: Ray tracing, FPGA implementation

Index Terms: I.3.1 [Hardware Architecture]: Graphics processors

1 Motivation

Only a few ray tracing systems have been fully implemented with *whitted-style* among several current interactive ray casting systems, as noted in [1]. This paper provides a full *whitted-style ray tracing* (WRT) accelerator on Xilinx Virtex 4 FPGA chip, called *WRTX*.

2 Prototype Implementation

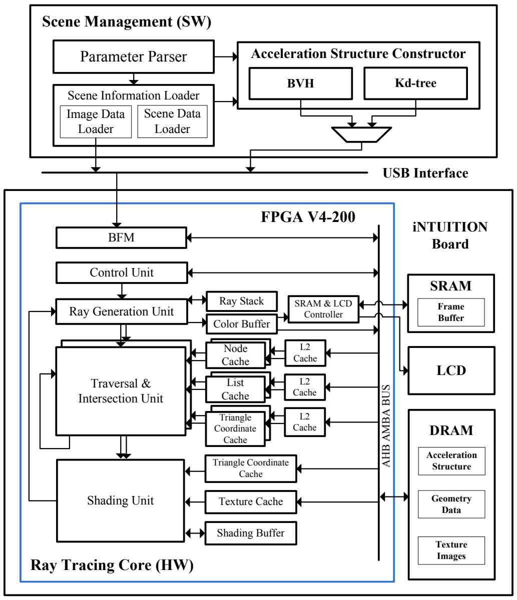

Figure 1: Overall System Architecture of *WRTX*.

Figure 1 shows the overall system architecture of *WRTX*. Scene management part in CPU builds and sends AS (acceleration structure) including geometry data and texture data to DRAM on FPGA board. Then, *WRTX* integrated in FPGA starts running. Final color value is written into frame buffer through color buffer. Current prototype *WRTX* operates at a speed of 48MHz and occupies about 1M logic gates with 0.6MB internal SRAM.

WRTX is implemented on Dynalith System's iNTUITION board which contains a Xilinx Virtex 4 FPGA, a TFT-LCD with 640 by 480 resolutions, a 512MByte DDR memory, 2MByte SRAM, and AHB bus at 24MHz with 32-bit width.

The core datapath part of *WRTX* consists of a ray generation unit, a T&I (traversal and intersection) unit, and a shading unit. A fully MIMD T&I unit to trace individual rays is the most important feature of *WRTX* not like current architectures with a SIMD traversal unit exploiting coherence by tracing bundles of rays. Due to the size limitation, current implementation equips with two T&I pipelines. In addition, *WRTX* includes several other outstanding features such as shadow ray culling, unified T&I unit, and colored shadow support. Full paper version of our work will be announced in the near future.

The memory system is composed of caches, buffers, and others to store material information. T&I units take two-level cache architecture. External memory is configured with SRAM for frame buffer and DRAM for AS, geometry data including triangle information, and texture images.

3 Performance Evaluation

Three benchmark scenes are selected from BART as shown in Figure 2. The number of lights is 6. They have a lot of secondary rays, and thus require relatively long rendering times.

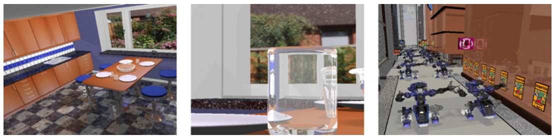

Figure 2: Three Benchmarks.

Table 1 tabulates the performance results of the FPGA implementation where SPF and RPS represent seconds per frame and rays per second, respectively. We achieve about 1.3M RPS and 90% of T&I pipeline utilization, which shows the proposed architecture can maintain high throughput rates regardless of ray types (e.g., for reflection and refraction).

Suppose *WRTX* equips with four T&I units and operates at 90MHz with fast SRAM in the same environment like SaarCOR, its performance may compete equally with SaarCOR. We are now implementing *WRTX* on iNEXT board with two Xilinx Virtex 5 FPGA chips and expect to achieve about 8 times performance improvement compared with the current implementation.

[Table 1] Performance Results of Current Implementation.

Scene (ray depth)	# of polygon	SPF	# of ray	RPS	T&I pipe. usage
Kitchen#1(0)	110K	1.7	2.1M	1.27M	85.16%
Kitchen#1(4)		3.5	3.5M	985K	85.58%
Kitchen#2(0)	110K	1.2	2.2M	1.75M	88.62%
Kitchen#2(10)		3.3	5.3M	1.58K	90.29%
Robot(0)	87K	1.5	2.2M	1.4M	96.98%
Robot(4)		3.7	4.6M	1.2M	97.79%

Acknowledgement

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References

[1] S. Boulos, D. Edwards, J. Lacewell, J. Kniss, J. Kautz, I. Wald, and P. Shirley, "Packet-based Whitted and Distribution Ray Tracing," Proc. Graphics Interface 07, May 2007, pp. 177-184.

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