

# CS/EE 5710/6710 -- CAD Assignment #2

Due Monday, September 14th, 5:00pm

Put assignments in the slot outside the SoC office

## Introduction

In this CAD assignment you will start physical (mask layout) design. You will implement a schematic and also the physical design layout that implements the same functionality as the schematic. Physical design is an exacting task, and you ALWAYS need to verify that your layout is correct. You will use two software tools to verify the correctness of your physical design. Design rule checking (DRC) software ensures that your layout obeys the myriad design rules that specify how the different layers interact. The physical design will then be verified structurally against the schematic (used as the specification). This is accomplished with the layout versus schematics (LVS) software. You will then run analog simulation using Spectre to generate analog waveforms from your design.

## Assignment Tasks

1. Design an inverter using transistors in a Composer schematic and simulate the inverter *both* with **Verilog**, and through the Analog Environment with **Spectre**. (This is covered in Chapters 3, 4, and 7 in the CAD book). You should also create a symbol view for this inverter. You may want to do this assignment within your **CAD1** library that you created in CAD assignment #1 rather than create a new library. You can use **nmos**, **pmos**, **vdd**, and **gnd** devices from either the **NCSU\_Analog\_Parts** or **UofU\_Analog\_Parts** libraries. The difference (as described in Chapter 3) is that the **NCSU** devices have zero delay when simulated by Verilog simulators, and the **UofU** devices have 0.1ns (100ps) of delay when simulated by Verilog simulators. Spectre simulations use detailed (analog) transistor models that give accurate delays based on device sizes, loads, and parasitic capacitances. This simulator produces results with analog waveforms.

Set the width of the devices in this inverter to be  $1.5\mu$  (1.5 microns) for the nmos and  $3\mu$  (3 microns) for the pmos. This will be our “unit sized” inverter for this class. Set the widths when you put the transistors in the schematic or use the “q” properties button to change parameters of transistors that are already in your schematic. The transistor length should be the default (600n which is 0.6 microns).

2. Draw the layout for the inverter in Virtuoso (covered in Chapter 5). For this layout, and for the NAND gate in part 3 you don't have to use the standard cell template in Chapter 6, but you should think about making the two layouts compatible in terms of (at least) the vdd and gnd connections. Run DRC and LVS to make sure you met the design rules, and that your layout does correspond to the transistor schematic in Part 1. Extract and simulate this inverter with Spectre (i.e. simulate the extracted view). Compare the waveform to the

analog waveform from Part 1. Note that you should draw the layout of the transistors to match the widths you used in the schematic.

3. Draw a layout for the two-input NAND gate that you designed in CAD assignment #1. Simulate that layout using Spectre (i.e. simulate the extracted view) and compare against the Verilog simulation from CAD #1. Verify the NAND gate layout with DRC and LVS against the transistor version from CAD #1. The transistor widths you should use are  $3\mu$  for both nmos and pmos (update the schematic to match these widths). Why did I pick these widths for the NAND gate?
4. Use the layout of the NAND gate and the layout of the inverter to design the layout version of the function from Cad #1 in Virtuoso. Modify the schematic for the function to use the inverter and NAND instead of only NAND gates. Remember that the function you're implementing is:

$$F = \overline{A}\overline{B} + \overline{A}C + \overline{B}C$$

In the layout you should include instances of the layout for the NAND and layout for the inverter in a new layout view, make the connections by drawing layout to connect them. Remember to connect vdd and gnd as well as the signals. Simulate this layout in Spectre. Verify with DRC and LVS against the modified schematic.

**Turn in hardcopies of:** All schematics, layouts, Verilog simulation testbenches and results, Spectre simulations (waveforms), and LVS logs. You should have three separate sets of documentation: your inverter, your NAND, and your F function.

**Note about LVS logs:** You don't need to print out the DRC logs. Note that the layout versus schematic (LVS) verification software will not run successfully unless you have already passed the design rule checking (DRC) software. So you just need to hand in the LVS logs. You can get to the LVS log in two ways.

- In the LVS window after you finish the LVS step, you need to press the **output** button to view the LVS log. In the LVS log window, do a **File ->save as** and save it to a file. Now you can print this file.
- Otherwise, in your `~/IC_CAD/cadence-f09/LVS` directory, you will find a file called **si.out**. This is your LVS log file. This is the same file as in the previous step.