Dynamic Source Filtering Sunglasses

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Computer Engineering Senior Project

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Table of Contents

Appendices

Introduction

The result of this project will be the development of intelligent sunglasses. The goal of the sunglasses is to dim bright lights while leaving a person's remaining field of view undisturbed. These sunglasses will be far superior to standard sunglasses in situations where the distribution of light is uneven. For example light is unevenly distributed when either driving into the sun or driving into oncoming headlights. The presence of bright lights causes the eye to adjust which makes the surrounding area darker by comparison. By dimming the bright spots, the eyes can remain dilated and continue to detect details from the surrounding area with much greater accuracy. The glasses will consist of four major components: clear Liquid Crystal Display (LCD) screens, digital cameras, microcontrollers/processors, and chassis. The design will consist of two separate systems that are functionally identical, where each system is dedicated to one eye.

Project Overview

The basic procedure the glasses will go through starts by the glasses using a camera to take a picture of what the viewer sees. The camera will stream that data to a microcontroller that will processes each pixel and determine whether dimming is necessary or not. If dimming is needed the microcontroller will calculate the position on the LCD screen that corresponds to the position of the bright spot. It will write data out to the LCD controller so that upon refreshing the screen the appropriate areas are dimmed. This will happen repeatedly and rapidly so that new lights are dimmed and light sources that have disappeared are no longer dimmed. The project can be split into three design categories: physical placement and design, hardware component design, and software design.

The physical placement will require all components to be mounted on a person's head so that they can look around. The main chassis will be more like a helmet than a pair of sun glasses. The LCD screens will be held in front of the viewers eyes so that a large portion of their field of view is through the screens. The cameras will be mounted pointing in the same direction as the viewer is facing and will be as close to the LCD screens as possible. The microcontroller and other components will be mounted on top of the helmet.

The hardware component design is based mainly on the minimum function requirements of the system. The LCD must not inhibit light transmission to the point of being impossible to see through and the system must have a quick response time to any change in lighting. Also, all parts must be able to communicate with one another efficiently. Special camera and LCD controllers will be designed to ensure both components can be used to their full potential in terms of response time.

The software design will require code to be programmed for an embedded microcontroller. The actual amount of code running must be minimized to ensure that the camera and screen can be serviced at their maximum data rates. Also, the code must be able to translate camera pixels to screen pixels as accurately as possible.

Design Constraints Overview

A critical aspect of the glasses' operation relies on the relative positions between the camera and the screen. The fundamental problem is that what the camera can see is going to be slightly different from what the person wearing the glasses can see. This phenomenon is referred to as parallax and can be used to measure distances, but in the sunglasses it will be perceived as a variable error that is dependent on distance. The error will be more apparent in objects close to the viewer and less apparent in objects at a large distance. The ideal location for the camera would be exactly in the same place as the eye; this is obviously unfeasible as the eye occupies that space. The next most ideal location would be in the center of the screen, or at least along the center line of the person's vision. This would make the center of the camera the same as the center of the screen; unfortunately, that would also be unfeasible as it would obscure the person's field of view. There is no perfect location for the camera to reside, but there are a few optimal locations given the previous physical constraints: above or below the screen in the center and to the left or right in the center. Each of those positions shares a center line with the human's eye and therefore minimizes either the side to side error or the up and down error (parallax). The camera that will be most effective for this project is above the screens in the center as that will be the most convenient for construction and the least likely spot to be accidentally damaged.

The cameras will be placed as close to the LCDs as possible, but it is hard to know the exact measurements before they are physically set in place. Because the error is so heavily dependent on the exact location of the cameras, a simulation was required so that the camera's location could be changed and the respective error observed. In the simulation the viewer's eye was represented three inches behind the screen and the camera was represented an inch above and an inch forward from the screen. In the simulation there is one light source that can be moved around. Figure 1 shows this simulation. To represent what the viewer can see, the light source is projected onto the LCD screen. The light source is also projected onto a ¼ inch screen at the camera location and superimposed on top of the image on the LCD screen. This is shown in Figure 2. From there, the change in error could be observed depending on where the light source was located. Beyond one mile, the error is nonexistent; the camera sees exactly what the viewer sees. The sun would fall into the category of objects that will have no error between what the camera sees and what the viewer sees. On objects 7 feet away, the error becomes so significant that what the viewer sees is in a completely different location than what the camera sees. To account for this the sunglasses will overscan what the camera sees to cover more area. The overscan cannot be too great because it will obscure vision. A width of 2 millimeters, or 10 pixels, darkened in a border around the bright object would not be obtrusive to vision and would allow the LCD glasses to block light sources as close as 12 feet accurately. If the cameras can be placed closer, that distance could be further decreased, but 12 feet is the worst case scenario.

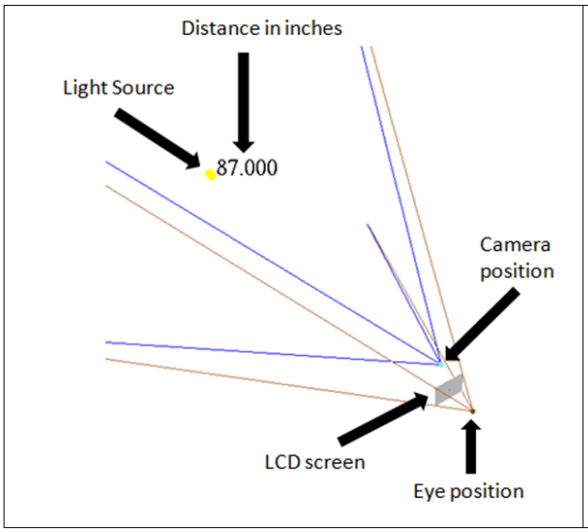


Figure 1: Glasses Operation Simulation. External Perspective

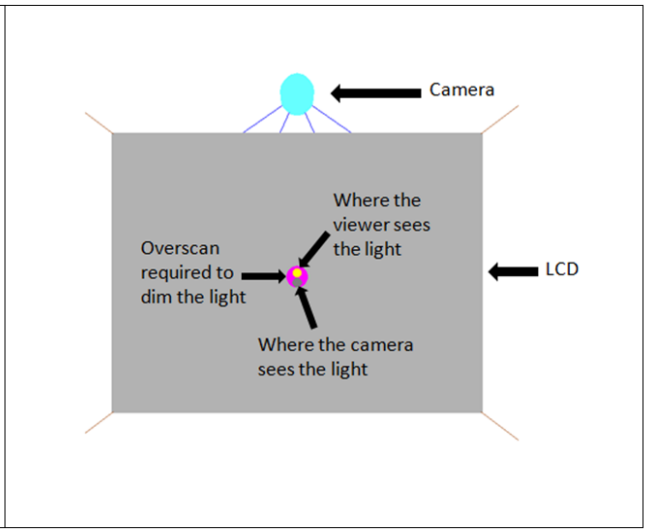


Figure 2: Glasses Operation Simulation Viewer's Perspective

The cameras will be sending data to the microcontroller that will process light sources. The microcontroller will then send the processed data to the LCD's. The LCD's will blot out any light sources above a certain threshold. This processing time could be an issue if it is longer than the time it takes for the pupil to react.

Pupil Response Time

A research study for the IEEE Engineering Medical Biology Society provided information on papillary response time. The group tested the papillary response time of subjects exposed to a single flash of light. The pupil response time was recorded for three seconds. The results are shown in Figure 3.

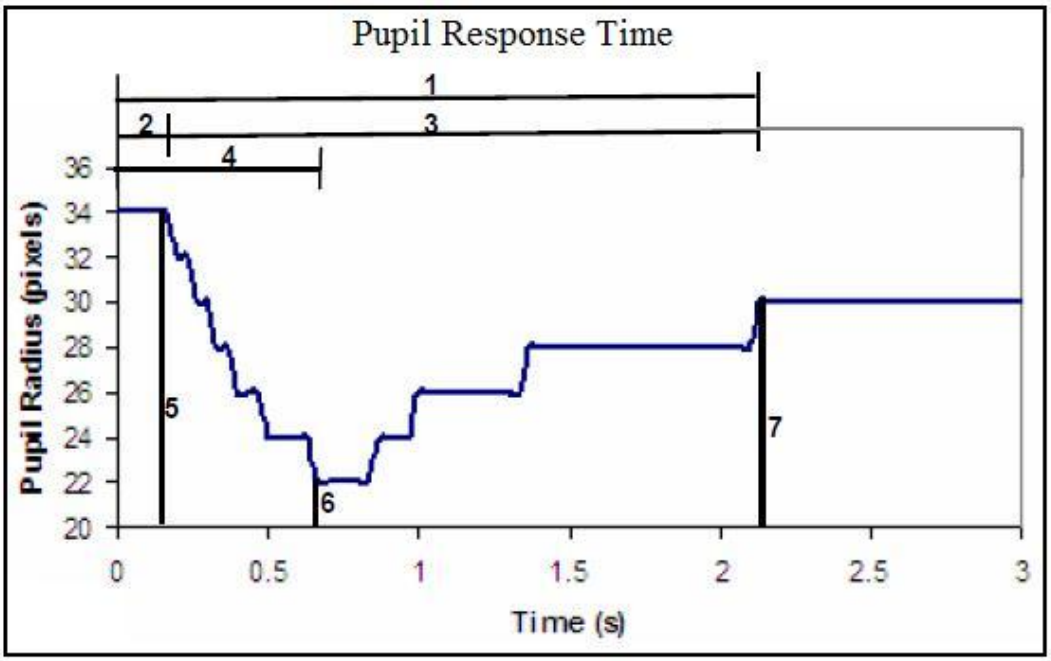


Fig. 3 Pupil response and parameters measure (1-Latency time to reach the plateau, 2-Latency time to the beginning of constriction, 3-Duration of constriction, 4-Latency time to maximum constriction, 5-Radius of pupil before flash, 6-Radius of pupil at maximum constriction, 7-Radius of pupil at teaching plateau).

The research group found that the latency time from the single flash exposure to the start of pupil constriction was (240±36ms). They also found that the time to total pupil constriction was between 0.6 and 0.7 seconds.

This data means that the code will have to be optimized so that the system processing time will fall below 240ms. The worst case scenario for the system's processing time will have to be shorter than the time it takes the eye to completely constrict which is between 0.6 and 0.7 seconds.

Bill of Materials

The sunglasses will be comprised of a few parts from different manufacturers. They will require LCDs, microcontroller boards, cameras, physical hardware for mounting, and various electrical components for interfacing. Table 1 shows the projected project costs.

Table 1: Projected Project Costs

Product	Quantity	Manufacturer	Price
LCD Screen PT0353224-A102	2	Palmtech	$50.00
Digital Camera C3188A-6018	3	OmniVision	$57.00
Spartan-3 FPGA Board	2	Digilent Inc.	$119.00
Physical Head Mounting Hardware	1	-	$20.00
Assorted Electrical Components	1	-	$20.00
Total			$549.00

The projected project cost is 549 dollars with some margin of error for miscellaneous components that may need to be purchased mid way through construction.
The LCD screens have already been acquired. They are the model PT0353224-A102 LCDs from Palmtech. The LCDs' measurements are approximately 70.08 x 52.56 (mm) and they have a resolution of 320 x 240 pixels. The screens are thin film transistor (TFT) transmissive displays which give enough clarity for our project, but not the ideal clarity for a commercial implementation.

Microcontroller

The microcontroller will be implemented using a field programmable gate array (FPGA). The FPGA will be purchased from Digilent Inc. in the Spartan-3 Board package. An FPGA design is essential for the sunglasses due to their ability to sustain multiple parallel processing pipelines in the same package. A standard microcontroller, such as the HCS12 from Freescale, does not have the data throughput required for the sunglasses. The FPGA contains a 50 MHz crystal oscillator with 20 Block Rams containing a total of 360kbits of Block Ram. This will allow for high processor speed as well as memory for the camera and LCD data buffers. Any required instructions can be implemented in the form of extra logic within the FPGA itself. An FPGA solution gives a greater range of flexibility and significantly cuts possible risks.

Digital Cameras

The digital cameras are the model C3188A-6018 manufactured by Omnivision. The cameras are capable of operating at a resolution of 320x240 pixels at 60 frames per second, and a resolution of 640x480 pixels at 30 frames per second. High frame rates are ideal for fast response time (preventing blindness), and high resolutions are desirable for wide angle viewing and increased accuracy. The cameras are capable of outputting data in the YCrCb format, a

format which allows information regarding the brightness value of a pixel to be separated easily. The sunglasses will only rely on the brightness (Y) values from the color vectors for processing. The use of a custom lens will also be investigated in order to further ease processing if required. A dark lens will replace the standard lens on the cameras to simplify the calculation of the threshold for dimming pixels. The cameras have already been acquired for the sunglasses.

Interfacing the Components

A few standard wires and adapters will be required to interface each component together. The LCDs, Cameras, and FPGAs all communicate using the 3.3v TTL standard which means the cost of interface components should remain low. There will also be a few knobs required for adjustments like eye distance that change from person to person. The total cost of miscellaneous electrical components is expected to be around 20 dollars.
The sunglasses will need physical mounting gear in the form of a helmet with brackets to hold the LCDs and cameras in a rigid position. It must also be wearable by most people for demonstration purposes. Most parts involved in the physical construction will be purchased at local department and hardware stores, but the estimated cost is around 20 dollars.

Interface Issues

Several interface issues have been discovered while performing initial project scoping. One such issue would definitely affect our ability to interface with our LCD screens. Our current LCD solution interfaces through 54 pin ribbon cable. Employing an FPGA solution as a substitute for a 3rd party microcontroller would allow a direct tie from each wire to an input pin to the FPGA. In order to possibly eliminate wire wrapping an adaptor would have to be found for the cable to make interfacing easier.

Another issue presents itself in the form of interfacing with a camera implementation. The current model camera looks very straightforward due to the fact that it also comes on a small controller board. However, the camera gives us the ability to acquire color images so it's also possible to perform image processing on color images and not just black and white. If so consideration would have to be applied to the extra bandwidth from the data, additional processing time for a more dynamic image, and time-constraints to allow quick dimming even with much larger data sets. Noise between all the wires that connect both the LCD and camera may also be an issue because of the sheer amount of wiring that will need to be connected.

Initial Schedule Flow

Due to the complex nature regarding the interactions of each component within the overall system, it has been decided to start early on the implementation to allow for unforeseen difficulties encountered during development. It is important that enough time is allocated to allow for a sufficient implementation of each component, debugging for each component, and system assembly implementation and debugging. Delegation of tasking to specific team members is further discussed in the Tentative Tasking section of this report.

Development will begin on the LCD component immediately as they are currently available to the project. An initial implementation solution of very basic functionality using the LCD is expected to be completed within 1.5 months, no later than the first week of July. The initial implementation will consist of at least the ability to correctly color all pixels using a prototype FPGA to send data to the LCDs. A more refined alpha version is expected to be completed in 4 months, no later than the last week of August. The alpha version must be a near complete prototype of the LCD interface. The ability to write a specific dimness value to a specific pixel on the LCD must be fully implemented. Additionally, the interface must be dynamic and allow the acceptance of specific commands from the microcontroller. Dana has accepted the main responsibility of implementing this component.

Development on the cameras will start at most within 1 month's time, no later than the first week of June. The camera modules have already been ordered and development is expected to begin as soon as they arrive. An initial component implementation is expected to be completed within 2 months. An initial solution will be characterized by the ability to receive data from the camera in the YCrCb format. The data need not be fully coherent, but should represent correct transmission of data. An alpha implementation is expected to be completed within 4 months, no later than the last week of August. An alpha version must be correctly able to write dimness values of every pixel to a correct corresponding location in memory. Also, the alpha build must be capable of accepting commands from the microcontroller. Torrey has accepted the main responsibility of implementing this component.

Design of a microcontroller solution will start within 1.5 month's time, no later than the 3rd week of June. The microcontrollers for the project have not been ordered yet but they shall be within the next week. An initial microcontroller implementation is expected to be completed within 2.5 months. The initial microcontroller will consist of a basic instruction set and a design mapping all the necessary requirements needed to interface with the camera and LCD. An alpha version of the microcontroller is expected to be completed within 4 months, no later than the last week of August. The alpha version must be capable of sending and receiving information from the LCD and camera using specific instructions optimized within the FPGA. Dan has accepted the main responsibility of implementing the microcontroller.

Finally, integration of all components into the system and debugging will finish the remaining months of the project. System integration of all components will begin in 5 months, no later than the first week of September. The integration will consist of ensuring the proper functionality of the system as a whole and debugging any errors found in the alpha implementations. In this phase, the inclusion of user IO will also be implemented in addition to any modifications needed by the system as determined by the team. A beta release is expected to be completed in 7 months, no later than the 2nd week of November. It would be very beneficial to try and finish all development and modifications a month ahead of schedule to allow enough time for debugging and difficulties that may be encountered during the duration of the project. Jason has accepted the main responsibility of overseeing the system integration with help from the team. Table 2 illustrates the expected schedule development to adhere to throughout the extent of the project.

Table 2: Expected Schedule Development

Time	Torrey	Jason	Dana	Dan
May				
June	Initial development of camera interface module.		Initial development of LCD interface solution.	Development of microcontroller Alpha build complete
July	Continued development of camera solution. Alpha version of camera modules complete.		Alpha version of LCD interface completed.	
August				
September	Begin initial system integration of all components. Begin system wide testing and debugging. Revise alpha implementations and refractor solutions when necessary. Assemble physical components and design layout for project. Implement user I/O control for specific modules. Make necessary efficiency changes time allowing. Complete near final beta release of each system individual system.			
October				
November	Complete final debug sprint and resolve and last minute issues with project. Finalize system stability and prepare final release. System release for demo day.			
December				

Tentative Tasking

In order to maximize time for testing and debugging our project, each component be will be designed concurrently whenever possible. Naturally, there are hardware and software components that need to be implemented before other parts can continue. The various aspects that comprise the project are assigned to the team as follows.

Dana will take the responsibility of interfacing to the LCD screens from a controller utilizing a simple state machine. The state machine will receive input from a screen buffer that will specify the appropriate shades for each pixel. The state machine will then output the specifications to each LCD independently. Basically, she will determine the format of the data and what constraints the data needs to be sent, clock speeds, bandwidth etc. Because it is possible that this aspect of the LCD interface will have many factors influencing it, Dan will also help Dana when needed.

Torrey will be responsible for implementing possible power converters for any future component we may need. We have specifically chosen all parts of our project to operate at the voltages our FPGA can provide specifically 5V and 3.3V. However, it's possible that we may need to implement a converter should we decide run our components off of a portable power source such as batteries. For this case, we will need converters to get the necessary voltages, in which case we will simply use DC to DC converters. Also, Torrey will interface with the user I/O in the form of knobs that control user settings on the glasses. Finally Torrey will also be responsible for interfacing with the Camera. Torrey will need to determine data transmission characteristics and receive data from the device. Jason will also help Torrey when needed.

Dan will determine the functionality of our microcontroller solution. He will be responsible for figuring out what exactly will be needed in order for the rest of the team to begin software implementations of their own modules. As mentioned before, Dan will also assist Dana in writing data to the LCD to color pixels.

Jason will be in charge of System Integrations between the major components of our system. He will work with the other team members on each segment they are in charge to gain of understanding of what will be needed to integrate the systems together into our final project. His role will also be the lead on the physical design aspect of the integration including the glasses/helmet that the system will be mounted on.

All team members will also assist others as they encounter problems on designated components. Members have simply been assigned specific components to implement in order to speed up development. After each module has been implemented, all team members will be responsible for designing the software components to tie all everything together. This shall include reading data from the camera to the microcontroller, analyzing the input, and determining the output to the LCD screens.

Testing

The error on the sunglasses will need to be small enough so that is doesn't obscure the vision of the wearer and yet it cannot miss light that requires coverage. The extreme of either situation would defeat the entire purpose of the sunglasses. The error will be measured using 3 main light sources: A 500 watt work lamp, truck headlights, and the sun. The work lamp will be used in lab testing as a variable distance light source to test the error on objects ranging from five to 30 feet away. The sun will represent a light source at infinity and should insure that the cameras can block enough light to completely protect one's eye. The Truck headlights will be used as a real world test case where the glasses performance at night can be measured. Ideally the glasses will be able to dim the headlights to a bearable level while still maintaining visibility in the rest of the field of view. Accurate dimming of a light source at a minimum of five feet away will be considered a complete success, accurate dimming at a minimum of 12 feet will be considered acceptable, and accurate dimming at infinity will be a minimum requirement for functional operation and demonstration.

Testing will be performed on the physical head gear that will be used to mount the LCDs, camera's, etc. This testing on the helmet or glasses apparatus will be on all 4 members of the group as well as several students chosen at random from either the Warnock or Merrill Engineering Buildings to ensure a good fit across multiple head sizes.

The LCDs will need to be tested to ensure that all pixels can be written to. Testing will vary between writing a solid color to the both LCDs and writing an inverting checkerboard to ensure that each pixel can be written to independently. Testing will also be composed of writing varying shades of grey to the screens.

Testing on the camera modules will consist of comparing specific image examples to the output using several light sources with varying intensities. The comparison will consist of either manual observation of images or a small debugging program used specifically for comparing pixel values of two similar images. The idea is to verify the camera sensitivity level to ensure that data sent to the microcontroller for processing will be fairly accurate in terms of specific areas for which to applying diming. Additionally, speed of the camera modules will be tested to ensure that images can be captured at a high enough frame rate to reduce sluggish real time performance for the system. The refresh rate will be tested at both the maximum and minimum capable resolutions of the cameras to ensure a best and worst case time threshold. Finally, system wide testing will encompass the majority of time allocated for testing the camera module as it will be necessary to observe the real time performance of the modules while the system is fully functionally.

Risks

Our current risk is viewing objects closer than ten feet away. An error in respective positions of light sources between the viewer's eye and the camera manifests itself when objects are closer than 500 feet. Since the error becomes significant below ten feet, the system would have to overscan what the camera sees.

Appendix A

References

Ferrari GL**,** Marques JL**,** Gandhi RA**,** Emery CJ**,** Tesfaye S**,** Heller SR**,** Schneider FK**,** Gamba HR**.,** **An approach to the assessment of diabetic neuropathy based on dynamic pupillometry.,** Conf Proc IEEE Eng Med Biol Soc. 2007;2007:557-60.

APPENDIX B - LCD Specs

PALM TECHNOLOGY CO., LTD.

The LCD(M) Specialist

CONTACT ADDRESS : 14F-15F, No.383, Yangming Rd.,Sanmin District, Kaohsiung City 807, Taiwan, R.O.C.
Tel: 886-7-3983966
Fax: 886-7-3982966
E-mail: sales@palmtech.com.tw

PART NO. : PT0353224-A102

FOR MESSRS. :

CONTENTS

3. General specifications

3.1 General specifications

It is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses the amorphous silicon TFT as a switching devices. This model is composed of a Transmissive type TFT-LCD Panel, a driver circuit and a back-light unit.

3.2 Features

- High image quality a-Si TFT LCD module.
- 16.7M color number.
- Support 24-bits(RGB) input mode
- High contrast, high brightness
- Low power consumption.

3.3 Applications

- PDA
- Hand-held Device

4. Mechanical data

No	Item	Specification	Remark
1	Type	Transmissive	--
2	Display Mode	Normally White	--
3	Pixel Element	a-Si TFT	--
4	Screen Size	3.5inch	--
5	Resolution	320(RGB) x240	--
6	Color Number	16.7M	--
7	Active Area	70.08 (W) x 52.56(H) (mm)	--
8	Dot Pitch	73 x 219 (μm)	--
9	Color Arrangement	RGB-stripe	--
10	Assembly Type	COG	--
11	Back Light	LED	--
12	Viewing Direction	6 o'clock	--
13	Weight	TBD	--
14	Module Dimension	76.9(W) x 63.9(H) x 4.75(D)	

5. Absolute maximum ratings

5.1 Electrical absolute maximum ratings

(1) TFT-LCD Panel Absolute Maximum Ratings

Ta=25℃ GND=0V

Item	Symbol	Condition	Standard Value		Unit	Remark
			Min.	Max.		
Power supply	VDDIO	VSS=0V	-0.3	4.0	V	--
Input Voltage	Vi	--	-0.3	5.0	V	--

* If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

(2) Back-Light Unit

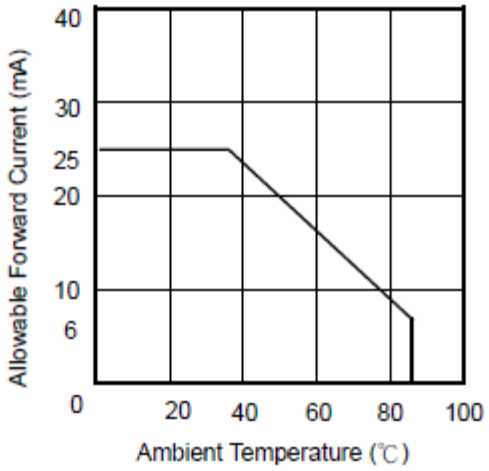
Ta=25℃

Item	Symbol	Min.	Max.	Unit	Remark
Current	I_B	--	(30)	mA	--

5.2 Environmental absolute maximum ratings

Item	Symbol	Min.	Max.	Unit	Remark
Operation temperature range	Top	-20	70	℃	Ambient
Storage temperature range	Tst	-30	80	℃	Ambient

(1) Corrosive gas environment is not acceptable.
(2) TFT-LCD color will change slightly depending on environment temperature. This phenomenon is reversible.
(3) Current reduction rate of LED backlight is according to the graph indicated below:



6. Electrical characteristics

(1)TFT-LCD Module

Ta =25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply voltage	VDDIO	(3.0)	(3.3)	(3.6)	V	--
Operating Current	IDD	--	(5.5)	(8.5)	mA	--
Vcom High Voltage	VCOMH	(2.5)	(3.6)	(4.5)	V	--
Vcom Low Voltage	VCOML	(-3.0)	(-2.4)	(0)	V	--

(2) Back-Light Unit

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Current	I_B	--	(20)	--	mA	--
Power Consumption	P_{BL}	--	(420)	--	mW	--

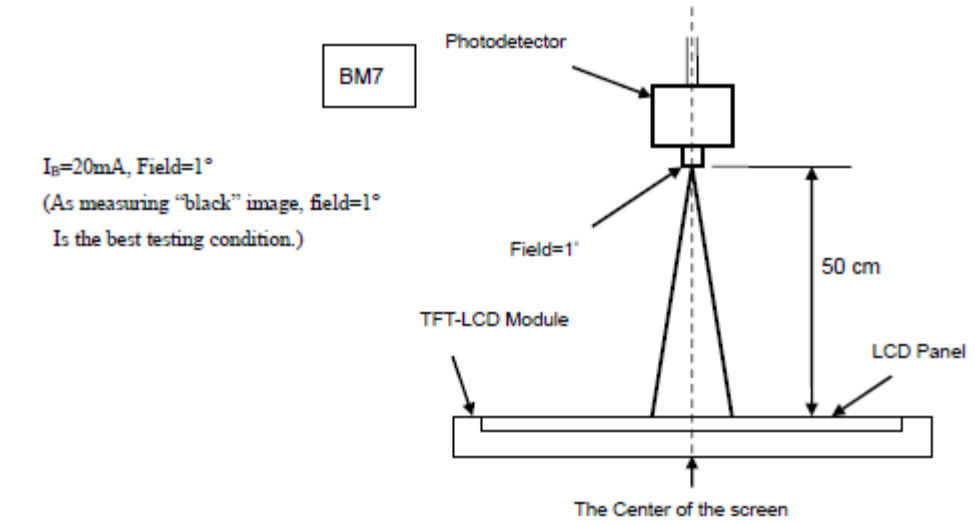
* Six LEDs is serial type

7. Optical characteristics

Ta = 25℃ , IB=20mA

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Brightness		B	θ=0° Normal viewing angle At the center of panel	(180)	(200)	--	cd/m^2	(1)
Contrast Ratio		C/R		(200)	(250)	--	--	(2)
Response Time		Tr+Tf		--	(50)	(70)	ms	(3)
Color chromaticity (CIE 1931)	White	Wx		(0.244)	(0.294)	(0.344)	--	--
		Wy		(0.259)	(0.309)	(0.359)		
	Red	Rx		(0.577)	(0.627)	(0.677)		
		Ry		(0.310)	(0.360)	(0.410)		
	Green	Gx		(0.282)	(0.332)	(0.382)		
		Gy		(0.506)	(0.556)	(0.606)		
	Blue	Bx		(0.091)	(0.141)	(0.191)		
		By		(0.040)	(0.090)	(0.140)		
Viewing Angle	Top	θ_U	CR≧10 Backlight On	--	(45)	--	Degrees	(4)
	Bottom	θ_D		--	(50)	--		
	Left	θ_L		--	(50)	--		
	Right	θ_R		--	(50)	--		
Uniformity		Un	θ=0° Normal viewing angle	(70)	--	--	%	(5)

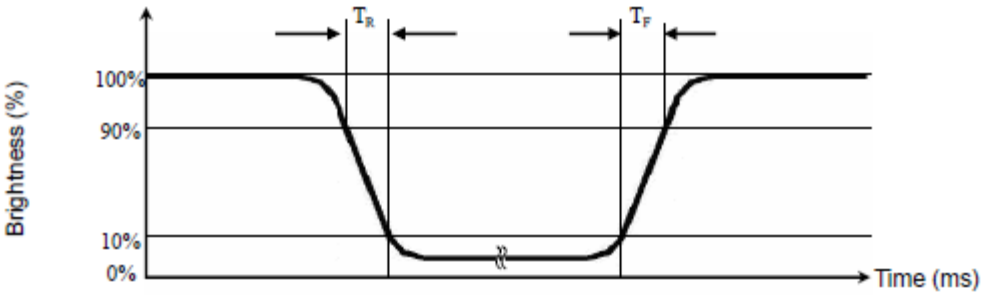
Note 1: The brightness test equipment setup



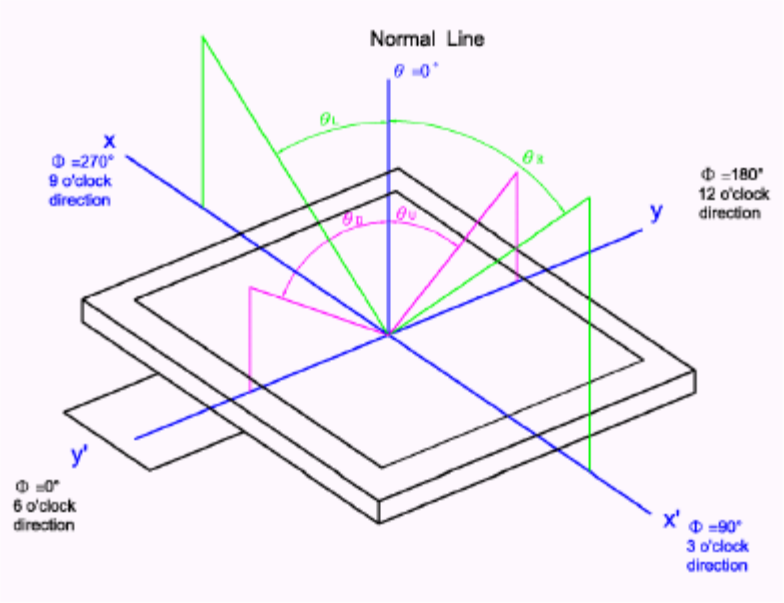
Note 2: Definition of contrast Ratio (C.R)

$$C.R = \frac{\text{Brightness When LCD is at "White" State}}{\text{Brightness When LCD is at "Black" State}}$$

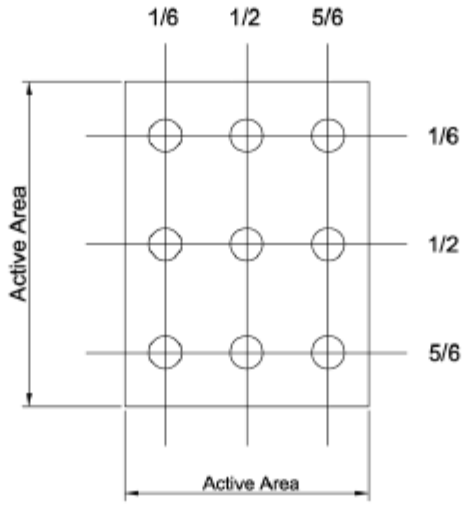
Note 3: Definition of response time



Note 4: Definition of viewing angle



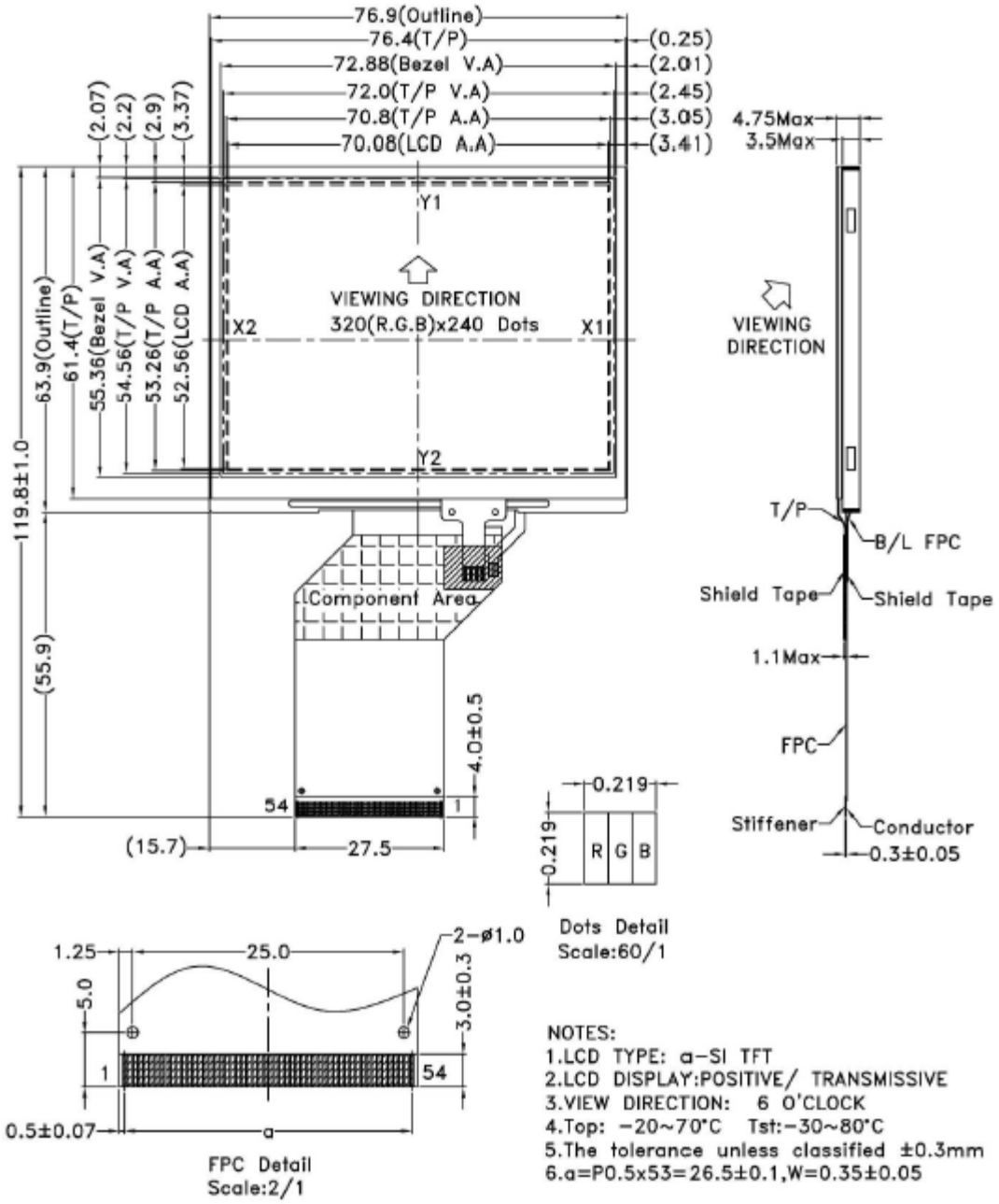
Note 5: Definition of uniformity (Un)



$$Un = \frac{Bmin}{Bmax} \times 100\%$$

PALM TECHNOLOGY CO., LTD. *Tel:886-7-3983966 Fax:886-7-3982966*	PT0353224-A102	VER:A	PAGE: 8/21

8. Outline dimension

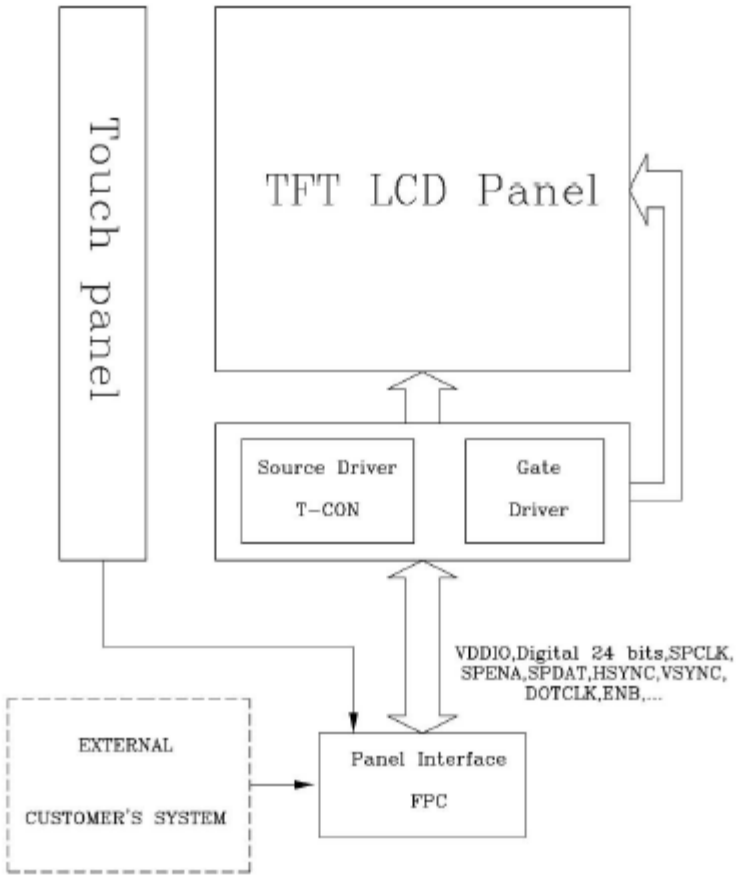


NOTES:
1.LCD TYPE: a-SI TFT
2.LCD DISPLAY:POSITIVE/ TRANSMISSIVE
3.VIEW DIRECTION: 6 O'CLOCK
4.Top: -20~70°C Tst:-30~80°C
5.The tolerance unless classified ±0.3mm
6.a=P0.5x53=26.5±0.1,W=0.35±0.05

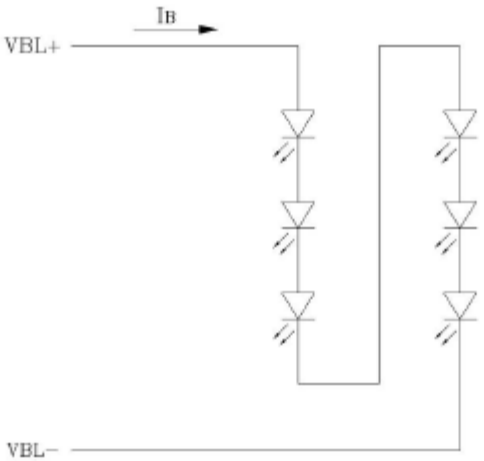
PALM TECHNOLOGY CO., LTD. Tel:886-7-3983966 Fax:886-7-3982966	PT0353224-A102	VER:A	PAGE: 9/21

9.Block diagram

9.1 TFT-LCD Module (Interface System Structure)



9.2 Back-light Unit



10. Input Terminal Pin Assignment

10.1 Input Signal & Power

Pin no	Symbol	Description	Remark
1	VBL-	Backlight LED ground	-
2	VBL-	Backlight LED ground	-
3	VBL+	Backlight LED power	-
4	VBL+	Backlight LED power	-
5	NC	NO CONNECTION	-
6	/RESET	Hardware reset	-
7	NC	NO CONNECTION	-
8	Y1	Touch panel TOP	-
9	X1	Touch panel RIGHT	-
10	Y2	Touch panel BOTTOM	-
11	X2	Touch panel LEFT	-
12	B0	Blue data bit 0	-
13	B1	Blue data bit 1	-
14	B2	Blue data bit 2	-
15	B3	Blue data bit 3	-
16	B4	Blue data bit 4	-
17	B5	Blue data bit 5	-
18	B6	Blue data bit 6	-
19	B7	Blue data bit 7	-
20	G0	Green data bit 0	-
21	G1	Green data bit 1	-
22	G2	Green data bit 2	-
23	G3	Green data bit 3	-
24	G4	Green data bit 4	-
25	G5	Green data bit 5	-
26	G6	Green data bit 6	-
27	G7	Green data bit 7	-
28	R0	Red data bit 0	-
29	R1	Red data bit 1	-
30	R2	Red data bit 2	-
31	R3	Red data bit 3	-
32	R4	Red data bit 4	-
33	R5	Red data bit 5	-

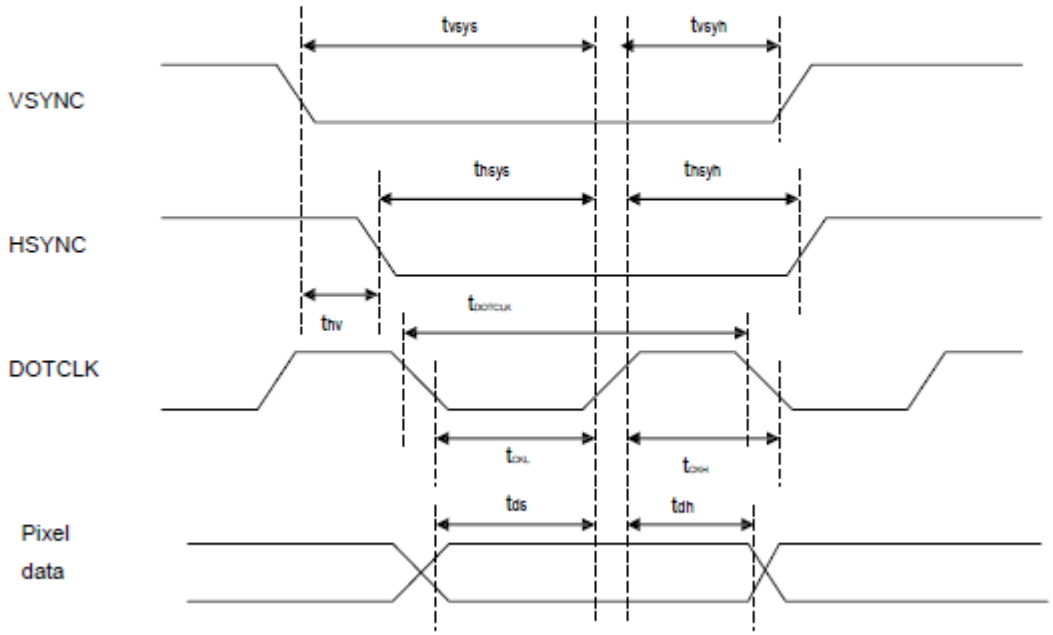
Pin no	Symbol	Description	Remark
34	R6	Red data bit 6	-
35	R7	Red data bit 7	-
36	HSYNC	Horizontal sync input	-
37	VSYNC	Vertical sync input	-
38	DOTCLK	Dot data clock	-
39	VDDIO	Digital power	-
40	VDDIO	Digital power	-
41	VDDIO	Digital power	-
42	VDDIO	Digital power	-
43	SPENA	SPI Interface Data Enable Signal	-
44	NC	NO CONNECTION	-
45	NC	NO CONNECTION	-
46	NC	NO CONNECTION	-
47	NC	NO CONNECTION	-
48	SHUT	Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low. - Connect to VDDIO for sleep mode - Connect to VSS for normal operating mode (Refer to Power Up Sequence)	-
49	SPCLK	SPI Interface Data Clock	-
50	SPDAT	SPI Interface Data	-
51	NC	NO CONNECTION	-
52	ENB	Data enable control	-
53	VSS	Ground	-
54	VSS	Ground	-

11. Basic Display Color and Gray Scale

Color			Input Color Data																							
			Red								Green								Blue							
			MSB							LSB	MSB							LSB	MSB							LSB
			R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)		1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta		1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red(0)	Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:		:	:	:	:	:	:	:	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(253)		1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	Bright	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green(0)	Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:		0	0	0	0	0	0	0	0	:	:	:	:	:	:	:	:	0	0	0	0	0	0	0	0
	Green (253)		0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	Bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Blue (0)	Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	:	:	:	:	:	:	:	:
	Blue (253)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	Bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

12. Timing Characteristics

12.1 Pixel timing

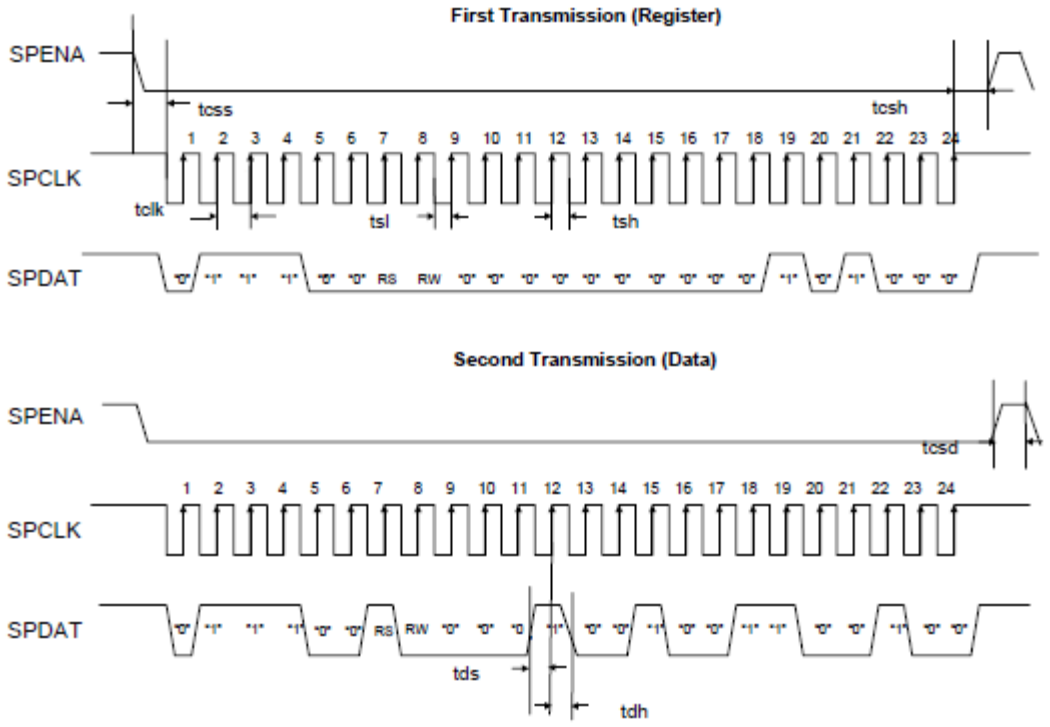


Characteristics	Symbol	Min		Typ		Max		Unit
		24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency	fDOTCLK	--	--	(6.5)	(19.5)	(10)	(30)	MHz
DOTCLK Period	tDOTCLK	(100)	(33.3)	(154)	(51.3)	--	--	ns
Vertical Sync Setup Time	tvsys	(20)	(10)	--	--	--	--	ns
Vertical Sync Hold Time	tvsyh	(20)	(10)	--	--	--	--	ns
Horizontal Sync Setup Time	thsys	(20)	(10)	--	--	--	--	ns
Horizontal Sync Hold Time	thsyh	(20)	(10)	--	--	--	--	ns
Phase difference of Sync Signal Falling Edge	thv	(1)		--		(240)		tDOTCLK
DOTCLK Low Period	tCKL	(50)	(15)	--	--	--	--	ns
DOTCLK High Period	tCKH	(50)	(15)	--	--	--	--	ns
Data Setup Time	tds	(12)	(10)	--	--	--	--	ns
Data hold Time	tdh	(12)	(10)	--	--	--	--	ns
Reset pulse width	tRES	(10)		--		--		µs

Note(1): External clock source must be provided to DOTCLK pin of HX8238-A.
The driver will not operate if absent of the clocking signal.

Note(2): The interface of this module can drive by digital 24-bit data

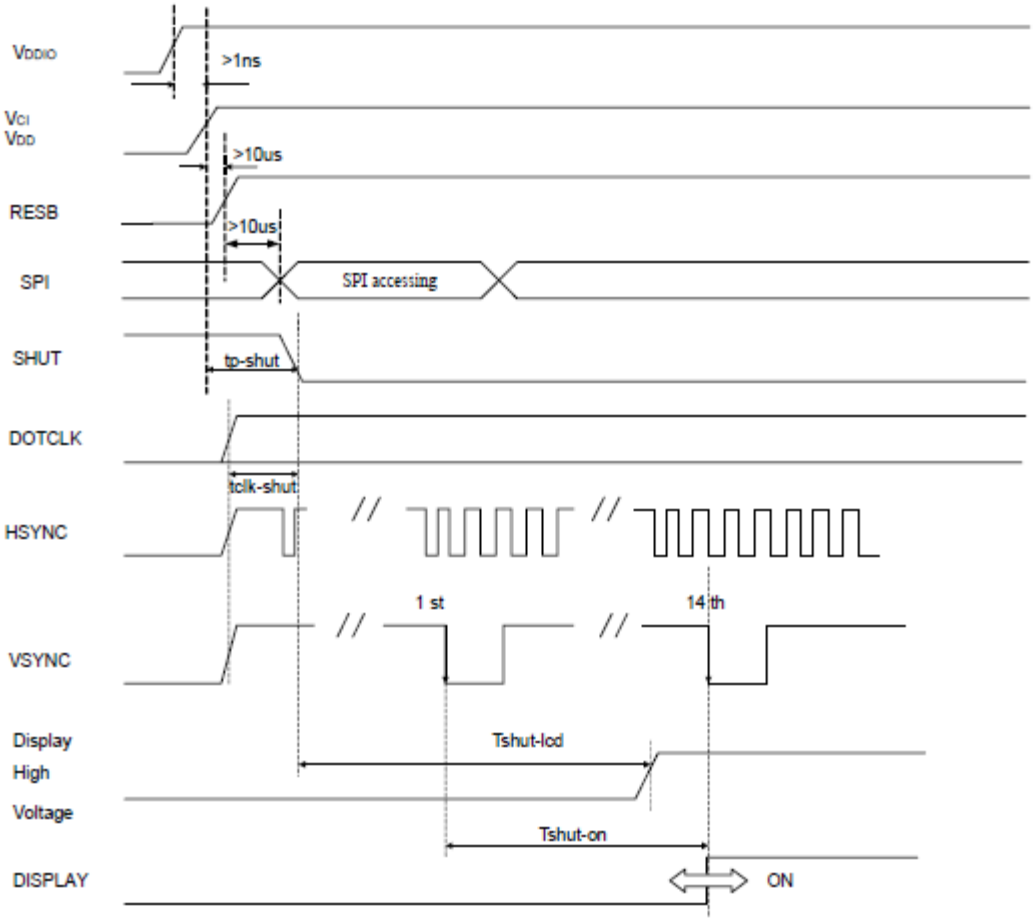
12.2 SPI interface timing diagram & transaction example



Note: The example transmit "0x1264h" to register R28h.
SPID connected to VSS.

Characteristics	Symbol	Min	Typ	Max	Unit
Serial Clock Frequency	fclk	--	--	(20)	MHz
Serial Clock Cycle Time	tclk	(50)	--	--	ns
Clock Low Width	tsl	(25)	--	--	ns
Clock High Width	tsh	(25)	--	--	ns
Chip Select Setup Time	tcss	(0)	--	--	ns
Chip Select Hold Time	tcsh	(10)	--	--	ns
Chip Select High Delay Time	tcsd	(20)	--	--	ns
Data Setup Time	tds	(5)	--	--	ns
Data Hold Time	tdh	(10)	--	--	ns

12.3 Power up sequence

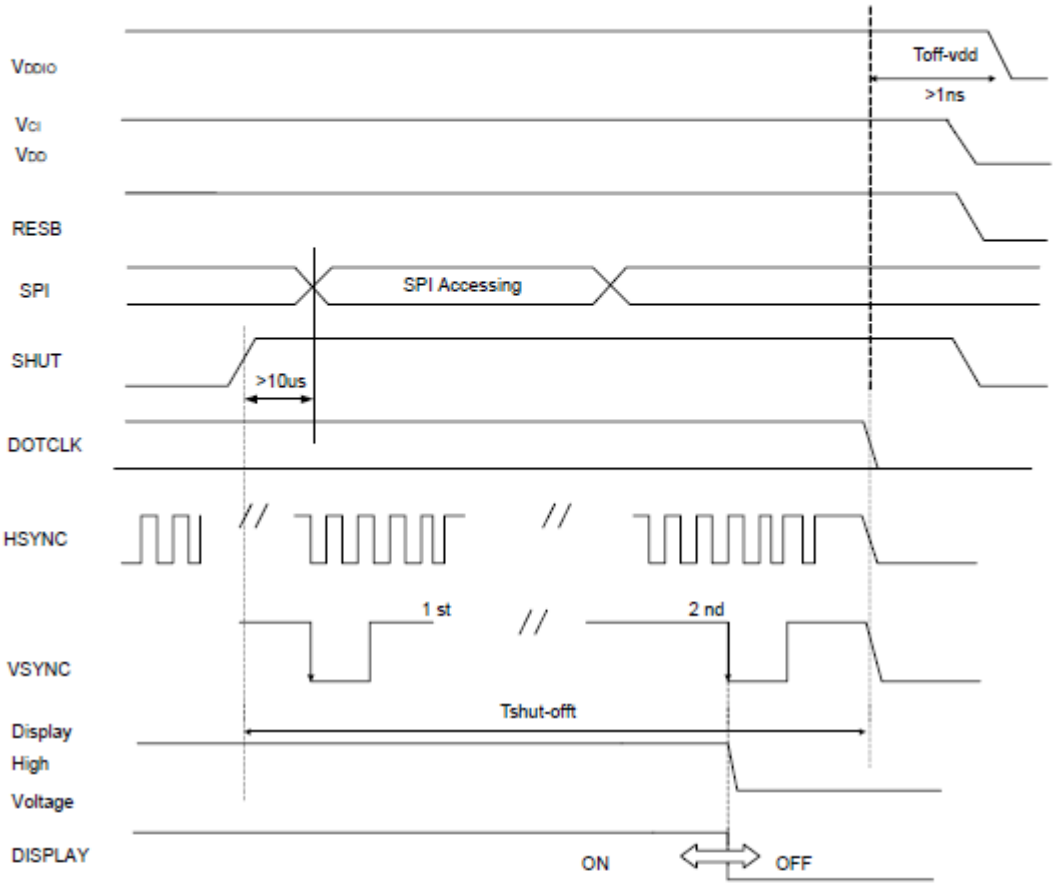


Characteristics	Symbol	Min	Typ	Max	Unit
VDDD / VDDIO on to falling edge of SHUT	tp-shut	(1)	--	--	μs
DOTCLK	tclk-shut	(1)	--	--	clk
Falling edge of SHUT to LCD power on	tshut-lcd	--	--	(128)	ms
Falling edge of SHUT to display start - 1 line: 408 clk - 1 frame: 262 line -DOTCLK = 6.5MHz	tshut-on	--	--	14	frame
		--	(166)	(232.4)	ms

Note(1): It is necessary to input DOTCLK before the falling edge of SHUT.
Display starts at 10th falling edge of VSTNC after the falling edge of SHUT.

Note(2):The voltage of VDD be boost from VDDIO.

12.4 Power down sequence



Characteristics	Symbol	Min	Typ	Max	Unit
Rising edge of SHUT to display off - 1 line: 408 clk - 1 frame: 262 line - DOTCLK = 6.5MHz	tshut-off	(2)	--	--	frame
		(33.4)	--	--	ms
Input-signal-off to VDDD / VDDIO off	toff-vdd	(1)	--	--	μs

Note(1): DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.

Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.

If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

Note(2): The voltage of VDD be boost from VDDIO.

APPENDIX C – Camera Specs

C3188A
1/3" Color Camera Module
With Digital Output

General Description

The C3188A is a 1/3" color camera module with digital output. It uses OmniVision's CMOS image sensor OV7620. Combining CMOS technology together with an easy to use digital interface makes C3188A a low cost solution for higher quality video image application.

The digital video port supplies a continuous 8/16 bit-wide image data stream. All camera functions, such as exposure, gamma, gain, white balance, color matrix, windowing, are programmable through I^2C interface.

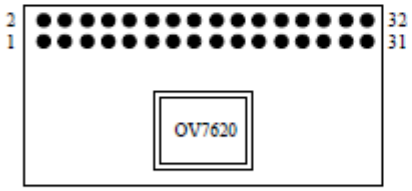
In combine with OV511+, USB controller chip, it will be easily form a USB camera for PC application.

Features:

326,688 pixels, VGA / CIF format
Small size : 40 x 28 mm
Lens: f=6mm (Optional)
8/16 bit video data : CCIR601, CCIR656, ZV port
Read out - progressive / interlace
Data format -YCrCb 4:2:2, GRB 4:2:2, RGB
I^2C interface
Built in 10bit 2 ch A/D converter
Electronic exposure / Gain / White balance control
Image enhancement - brightness, contrast, gamma, saturation, sharpness, window, etc
Internal / external synchronization scheme
Frame exposure / line exposure option
Wide dynamic range, anti blooming, zero smearing
Single 5V operation
Low power consumption (<120mW)
Monochrome composite video signal output (60Hz)

Specification

Imager	OV7620, CMOS image sensor
Array Size	664x492 pixels
Pixel size	7.6 x 7.6 µm
Scanning	Progressive / interlace
Effective image area	4.86mm x 3.64mm
Electronic Exposure	500:1
Gamma Correction	128 curve settings
S/N Ratio	>48dB
Min Illumination	2.5lux @F1.4
Operation Voltage	5 VDC
Operation Current	120mW Active 10 µW Standby
Lens (Optional)	f6mm, F1.6



PCB Layout (Top view)

Pin Description

1~8	Y0~Y7	Digital output Y Bus.
9	PWDN	Power down mode
10	RST	Reset
11	SDA	I^2C Serial data
12	FODD	Odd Field flag
13	SCL	I^2C Serial clock input
14	HREF	Horizontal window reference output
15	AGND	Analog Ground
16	VSYN	Vertical Sync output
17	AGND	Analog Ground
18	PCLK	Pixel clock output
19	EXCLK	External clock input (need to remove crystal)
20	VCC	Power Supply 5VDC
21	AGND	Analog Ground
22	VCC	Power Supply 5VDC
23~30	UV0-UV7	Digital output UV bus.
31	GND	Common ground
32	VTO	Video Analog Output (75Ω monochrome)

Application Example

- Video Conferencing
- PC Multimedia
- Video Phone
- Video Mail
- Still Image
- Machine Vision
- Process control

Note: Evaluation Board is available for C3188A

To order contact: Electronics123.com, Inc. web: www.electronics123.com e-mail: general@electronics123.com

APPENDIX D – Microcontroller Specs

Extended Spartan-3A Family
Optimized for Lowest Total Cost

	Part Number	XC3S50A / AN	XC3S200A / AN	XC3S400A / AN	XC3S700A / AN	XC3S1400A / AN	XC3SD1800A	XC3SD3400A
Logic Resources	System Gates [1]	50K	200K	400K	700K	1400K	1800K	3400K
	Slices [2]	704	1,792	3,584	5,888	11,264	16,640	23,872
	Logic Cells	1,584	4,032	8,064	13,248	25,344	37,440	53,712
	CLB Flip-Flops	1,408	3,584	7,168	11,776	22,528	33,280	47,744
Memory Resources	Maximum Distributed RAM (Kbits)	11	28	56	92	176	260	373
	Block RAM Blocks	3	16	20	20	32	84	126
	Total Block RAM (Kbits)	54	288	360	360	576	1,512	2,268
Non-Volatile Capability	Single Chip Option	Yes	Yes	Yes	Yes	Yes	No	No
	User Flash (Kbits) [3]	– / 627	– / 3,054	– / 2,380	– / 5,779	– / 12,251	—	—
Clock Resources	Digital Clock Managers (DCMs)	2	4	4	8	8	8	8
I/O Resources	Maximum Single Ended I/Os	144 / 108	248 / 195	311	372	502	519	469
	Maximum Differential I/O Pairs	64 / 50	112 / 90	142	165	227	227	213
	I/O Standards Supported	LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64bit 33MHz, PCI 3.3V 64bit/66MHz, PCI-X 3.3V, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, SSTL18 Class II, Bus LVDS, LVDS25 & 33, LVPECL25 & 33, Mini-LVDS25 & 33, RSDS25 & 33, TMDS33, PPDS25 & 33						
Embedded Hard IP Resources	Multipliers/DSP48A Blocks	3	16	20	20	32	84 [4]	126 [4]
	Device DNA Security	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Speed Grades	Commercial	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5
	Industrial	-4	-4	-4	-4	-4	-4 [5]	-4 [5]
Configuration	Configuration Memory Bits (Kbits)	0.4	1.2	1.9	2.7	4.8	8.2	11.7

Package [6]	Size	Maximum User I/Os						
VQFP Packages (VQ): very thin QFP (0.5 mm lead spacing)								
VQ100	16 x 16 mm	68 / – [7]	68 / – [7]					
TQFP Packages (TQ): thin QFP (0.5 mm lead spacing)								
TQ144	22 x 22 mm	108 / 108						
FGA Packages (FT): wire-bond fine-pitch thin BGA (1.0 mm ball spacing)								
FT256	17 x 17 mm	144 / – [7]	195 / 195	195 / – [7]	161 / – [7]	161 / – [7]		
Chip Scale Packages (CS): wire-bond chip-scale BGA (0.8 mm ball spacing)								
CS484	19 x 19 mm						309 [5]	309 [5]
FGA Packages (FG): wire-bond fine-pitch BGA (1.0 mm ball spacing)								
FG320	19 x 19 mm		248 / – [7]	251 / – [7]				
FG400	21 x 21 mm			311 / 311	311 / – [7]			
FG484	23 x 23 mm				372 / 372	375 / – [7]		
FG676	27 x 27 mm					502 / 502	519	469

Notes: 1. System Gates include 20%-30% of CLBs used as RAMs 2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic 3. Spartan-3AN User Flash is the space left in the on-chip Flash after a portion is used to store configuration bitstream 4. Integrated in the DSP48A slices (Advanced Multiply Accumulate element) 5. The L low-power option is exclusively available in CS(G)484 package and Industrial temperature range 6. All products available Pb-free and RoHS-Compliant, check datasheet for Pb package availability 7. Package not available in non-volatile Spartan-3AN family