This lab is a short lab that builds on the infrastructure from Lab3. The main things to take away from this lab are a better understanding of writing Verilog descriptions (using always, case, conditionals, etc), and a better understanding of signed and unsigned arithmetic.

Using two four-bit inputs, similar to Lab3, as inputs A[3:0] and B[3:0], design and simulate a circuit to compute three bits of output:

- L: This signal will be high if B < A as unsigned numbers
- N: This signal will be high if B<A as signed numbers
- E: This signal will be high if A==B

Use Verilog to define your circuit. Simulate the circuit exhaustively with a self-checking testbench. Hand in the Verilog code for the comparison circuit, the Verilog code for the testbench, the output of the simulation, and a representative piece of the output waveform. Also report how many BELS your circuit used, the worst-case delay path, and the delay of that path as reported in the synthesis report.

Note that there is no wiring or circuit demo for this lab. It is just Verilog simulation of a circuit. But, you should go through the synthesis process after it simulates so that you can report on how many BELS your circuit would use if you mapped it to the Xilinx part.