74HC/HCT283
4-bit binary full adder with fast carry

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

December 1990

File under Integrated Circuits, IC06
## FEATURES
- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal look-ahead carry
- Output capability: standard
- $I_{CC}$ category: MSI

## GENERAL DESCRIPTION
The 74HC/HCT283 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT283 add two 4-bit binary words ($A_n$ plus $B_n$) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1$ to $\Sigma_4$) and the out-going carry ($C_{OUT}$) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the “283” can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic); see function table. In case of all active LOW operands the results $\Sigma_1$ to $\Sigma_4$ and $C_{OUT}$ should be interpreted also as active LOW. With active HIGH inputs, $C_{IN}$ must be held LOW when no “carry in” is intended. Interchanging inputs of equal weight does not affect the operation, thus $C_{IN}$, $A_1$, $B_1$ can be assigned arbitrarily to pins 5, 6, 7, etc.

See the “583” for the BCD version.

## QUICK REFERENCE DATA

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>HC</th>
<th>HCT</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{PHL}/I_{PLH}$</td>
<td>propagation delay</td>
<td>$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$</td>
<td>16</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>$C_{IN}$ to $\Sigma_1$</td>
<td></td>
<td></td>
<td>18</td>
<td>21</td>
<td>ns</td>
</tr>
<tr>
<td>$C_{IN}$ to $\Sigma_2$</td>
<td></td>
<td></td>
<td>20</td>
<td>23</td>
<td>ns</td>
</tr>
<tr>
<td>$C_{IN}$ to $\Sigma_3$</td>
<td></td>
<td></td>
<td>23</td>
<td>27</td>
<td>ns</td>
</tr>
<tr>
<td>$C_{IN}$ to $\Sigma_4$</td>
<td></td>
<td></td>
<td>21</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>$A_n$ or $B_n$ to $\Sigma_n$</td>
<td></td>
<td></td>
<td>20</td>
<td>23</td>
<td>ns</td>
</tr>
<tr>
<td>$C_{IN}$ to $C_{OUT}$</td>
<td></td>
<td></td>
<td>20</td>
<td>24</td>
<td>ns</td>
</tr>
<tr>
<td>$A_n$ or $B_n$ to $C_{OUT}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_I$</td>
<td>input capacitance</td>
<td>3.5</td>
<td>3.5</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>$C_{PD}$</td>
<td>power dissipation capacitance per package</td>
<td>notes 1 and 2</td>
<td>88</td>
<td>92</td>
<td>pF</td>
</tr>
</tbody>
</table>

### Notes
1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in $\mu$W):
   $$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
   where:
   - $f_i$ = input frequency in MHz
   - $f_o$ = output frequency in MHz
   - $\sum (C_L \times V_{CC}^2 \times f_o) = $ sum of outputs
   - $C_L$ = output load capacitance in pF
   - $V_{CC}$ = supply voltage in V
2. For HC the condition is $V_I$ = GND to $V_{CC}$
   For HCT the condition is $V_I$ = GND to $V_{CC} - 1.5 \text{ V}$
4-bit binary full adder with fast carry  74HC/HCT283

ORDERING INFORMATION
See "74HC/HCT/HCU/HCMOS Logic Package Information".

PIN DESCRIPTION

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>SYMBOL</th>
<th>NAME AND FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>4, 1, 13, 10</td>
<td>Σ₁ to Σ₄</td>
<td>sum outputs</td>
</tr>
<tr>
<td>5, 3, 14, 12</td>
<td>A₁ to A₄</td>
<td>A operand inputs</td>
</tr>
<tr>
<td>6, 2, 15, 11</td>
<td>B₁ to B₄</td>
<td>B operand inputs</td>
</tr>
<tr>
<td>7</td>
<td>Cᵢn</td>
<td>carry input</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>9</td>
<td>Cᵪut</td>
<td>carry output</td>
</tr>
<tr>
<td>16</td>
<td>VCC</td>
<td>positive supply voltage</td>
</tr>
</tbody>
</table>

Fig.1 Pin configuration.
Fig.2 Logic symbol.
Fig.3 IEC logic symbol.
**4-bit binary full adder with fast carry**

**74HC/HCT283**

![Functional diagram](image)

**FUNCTION TABLE**

| PINS | C<sub>IN</sub> | A<sub>1</sub> | A<sub>2</sub> | A<sub>3</sub> | A<sub>4</sub> | B<sub>1</sub> | B<sub>2</sub> | B<sub>3</sub> | B<sub>4</sub> | Σ<sub>1</sub> | Σ<sub>2</sub> | Σ<sub>3</sub> | Σ<sub>4</sub> | C<sub>OUT</sub> | EXAMPLE<sup>(2)</sup> |
|------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|----------------|
| logic levels | L | L | H | L | H | H | L | H | H | H | L | L | H | |
| active HIGH | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | | (3) |
| active LOW  | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | | (4) |

**Note**

1. **H** = HIGH voltage level
   
2. **L** = LOW voltage level

2. **example**
   
   1001
   1010
   ------
   10011

3. for active HIGH, example = (9 + 10 = 19)

4. for active LOW, example = (carry + 6 + 5 = 12)
4-bit binary full adder with fast carry

Fig.5 Logic diagram.
4-bit binary full adder with fast carry

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

$I_{CC}$ category: MSI

**AC CHARACTERISTICS FOR 74HC**

$GND = 0\ V; t_r = t_f = 6\ ns; C_L = 50\ pF$

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>$T_{amb} (°C)$</th>
<th>UNIT</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>+25</td>
<td>–40 to +85</td>
<td>–40 to +125</td>
</tr>
<tr>
<td></td>
<td></td>
<td>min.</td>
<td>typ.</td>
<td>max.</td>
</tr>
<tr>
<td>$t_{PHL}/t_{PLH}$</td>
<td>propagation delay $C_{IN}$ to $\Sigma_1$</td>
<td>52</td>
<td>160</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>19</td>
<td>32</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>27</td>
<td>34</td>
</tr>
<tr>
<td>$t_{PHL}/t_{PLH}$</td>
<td>propagation delay $C_{IN}$ to $\Sigma_2$</td>
<td>58</td>
<td>180</td>
<td>225</td>
</tr>
<tr>
<td></td>
<td></td>
<td>21</td>
<td>36</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td></td>
<td>17</td>
<td>31</td>
<td>38</td>
</tr>
<tr>
<td>$t_{PHL}/t_{PLH}$</td>
<td>propagation delay $C_{IN}$ to $\Sigma_3$</td>
<td>63</td>
<td>195</td>
<td>245</td>
</tr>
<tr>
<td></td>
<td></td>
<td>23</td>
<td>39</td>
<td>49</td>
</tr>
<tr>
<td></td>
<td></td>
<td>18</td>
<td>33</td>
<td>42</td>
</tr>
<tr>
<td>$t_{PHL}/t_{PLH}$</td>
<td>propagation delay $C_{IN}$ to $\Sigma_4$</td>
<td>74</td>
<td>230</td>
<td>290</td>
</tr>
<tr>
<td></td>
<td></td>
<td>27</td>
<td>46</td>
<td>58</td>
</tr>
<tr>
<td></td>
<td></td>
<td>22</td>
<td>39</td>
<td>49</td>
</tr>
<tr>
<td>$t_{PHL}/t_{PLH}$</td>
<td>propagation delay $A_n$ or $B_n$ to $\Sigma_n$</td>
<td>69</td>
<td>210</td>
<td>265</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25</td>
<td>42</td>
<td>53</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20</td>
<td>36</td>
<td>45</td>
</tr>
<tr>
<td>$t_{PHL}/t_{PLH}$</td>
<td>propagation delay $C_{IN}$ to $C_{OUT}$</td>
<td>63</td>
<td>195</td>
<td>245</td>
</tr>
<tr>
<td></td>
<td></td>
<td>23</td>
<td>39</td>
<td>49</td>
</tr>
<tr>
<td></td>
<td></td>
<td>18</td>
<td>33</td>
<td>42</td>
</tr>
<tr>
<td>$t_{PHL}/t_{PLH}$</td>
<td>propagation delay $A_n$ or $B_n$ to $C_{OUT}$</td>
<td>63</td>
<td>195</td>
<td>245</td>
</tr>
<tr>
<td></td>
<td></td>
<td>23</td>
<td>39</td>
<td>49</td>
</tr>
<tr>
<td></td>
<td></td>
<td>18</td>
<td>33</td>
<td>42</td>
</tr>
<tr>
<td>$t_{THL}/t_{TLH}$</td>
<td>output transition time</td>
<td>19</td>
<td>75</td>
<td>95</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7</td>
<td>15</td>
<td>19</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6</td>
<td>13</td>
<td>16</td>
</tr>
</tbody>
</table>
4-bit binary full adder with fast carry 74HC/HCT283

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

<table>
<thead>
<tr>
<th>INPUT</th>
<th>UNIT LOAD COEFFICIENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{IN}</td>
<td>1.50</td>
</tr>
<tr>
<td>B_{2}, A_{2}, A_{1}</td>
<td>1.00</td>
</tr>
<tr>
<td>B_{1}</td>
<td>0.40</td>
</tr>
<tr>
<td>B_{4}, A_{4}, A_{3}, B_{3}</td>
<td>0.50</td>
</tr>
</tbody>
</table>

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_{r} = t_{f} = 6 ns; C_{L} = 50 pF

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>T_{amb} (°C)</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>+25</td>
<td>-40 to +85</td>
</tr>
<tr>
<td></td>
<td></td>
<td>min. typ.</td>
<td>min. max.</td>
</tr>
<tr>
<td>I_{PHL} / I_{PLH}</td>
<td>propagation delay C_{IN} to \Sigma_1</td>
<td>18 31</td>
<td>39 47</td>
</tr>
<tr>
<td>I_{PHL} / I_{PLH}</td>
<td>propagation delay C_{IN} to \Sigma_2</td>
<td>25 43</td>
<td>54 65</td>
</tr>
<tr>
<td>I_{PHL} / I_{PLH}</td>
<td>propagation delay C_{IN} to \Sigma_3</td>
<td>27 46</td>
<td>58 69</td>
</tr>
<tr>
<td>I_{PHL} / I_{PLH}</td>
<td>propagation delay C_{IN} to \Sigma_4</td>
<td>31 53</td>
<td>66 80</td>
</tr>
<tr>
<td>I_{PHL} / I_{PLH}</td>
<td>propagation delay A_n or B_n to \Sigma_n</td>
<td>29 49</td>
<td>61 74</td>
</tr>
<tr>
<td>I_{PHL} / I_{PLH}</td>
<td>propagation delay C_{IN} to C_{OUT}</td>
<td>27 46</td>
<td>58 69</td>
</tr>
<tr>
<td>I_{PHL} / I_{PLH}</td>
<td>propagation delay A_n or B_n to C_{OUT}</td>
<td>28 48</td>
<td>60 72</td>
</tr>
<tr>
<td>I_{THL} / I_{TLH}</td>
<td>output transition time</td>
<td>7 15 19 22</td>
<td>ns 4.5 Fig.6</td>
</tr>
</tbody>
</table>

December 1990
4-bit binary full adder with fast carry  74HC/HCT283

AC WAVEFORMS

Fig. 6 Waveforms showing the inputs (C\textsubscript{IN}, A\textsubscript{n}, B\textsubscript{n}) to the outputs (∑\textsubscript{n}, C\textsubscript{OUT}) propagation delays and the output transition times.

APPLICATION INFORMATION

Fig. 7 3-bit adder.

Fig. 8 2-bit and 1-bit adder.

Fig. 9 5-input encoder.

Fig. 10 5-input majority gate.

Notes to Figs  7 to 10

Figure 7 shows a 3-bit adder using the “283”. Tying the operand inputs of the fourth adder (A\textsubscript{3}, B\textsubscript{3}) LOW makes ∑\textsubscript{3} dependent on, and equal to, the carry from the third adder. Based on the same principle, Figure 8 shows a method of dividing the “283” into a 2-bit and 1-bit adder. The third stage adder (A\textsubscript{2}, B\textsubscript{2}, ∑\textsubscript{2}) is used simply as means of transferring the carry into the fourth stage (via A\textsubscript{2} and B\textsubscript{2}) and transferring the carry from the second stage on ∑\textsubscript{2}. Note that as long as A\textsubscript{2} and B\textsubscript{2} are the same, HIGH or LOW, they do not influence ∑\textsubscript{2}. Similarly, when A\textsubscript{2} and B\textsubscript{2} are the same, the carry into the third stage does not influence the carry out of the third stage. Figure 9 shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs ∑\textsubscript{0}, ∑\textsubscript{1}, and ∑\textsubscript{2} produce a binary number equal to the number inputs (I\textsubscript{1} to I\textsubscript{5}) that are HIGH. Figure 10 shows a method of implementing a 5-input majority gate. When three or more inputs (I\textsubscript{1} to I\textsubscript{5}) are HIGH, the output M\textsubscript{5} is HIGH.

PACKAGE OUTLINES

See “74HC/HCT/HCU/HCMOS Logic Package Outlines”.

December 1990  8