

Proper Grounding Is Critical For High-Speed Systems

BY WALT KESTER AND JAMES BRYANT

GROUND planes not only act as a low-impedance return path for high-frequency currents but also minimize electromagnetic-interference (EMI) and RF-interference (RFI) emissions. Due to the shielding action of the ground plane, a circuit's susceptibility to external EMI/RFI is also reduced. All integrated-circuit (IC) ground pins should be soldered directly to the ground plane to minimize series inductance. Power-supply pins should be decoupled to the ground plane using low-inductance ceramic surface-mount capacitors. If through-hole mounted ceramic capacitors must be used, their leads should be less than 1 mm. Ferrite beads may be also required.

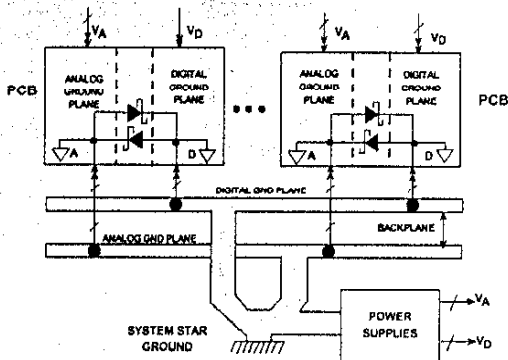
An effective ground plane allows the impedance of printed-circuit-board (PCB) traces to be controlled, and high-frequency signals can be terminated in the characteristic impedance of the trace to minimize reflections. Each PCB in a system should have at least one complete layer dedicated to the ground plane. Ideally, a double-

THE IMPORTANCE OF MAINTAINING A LOW-IMPEDANCE, LARGE-AREA GROUND PLANE IS CRITICAL TO MOST HIGH-SPEED ANALOG CIRCUITS.

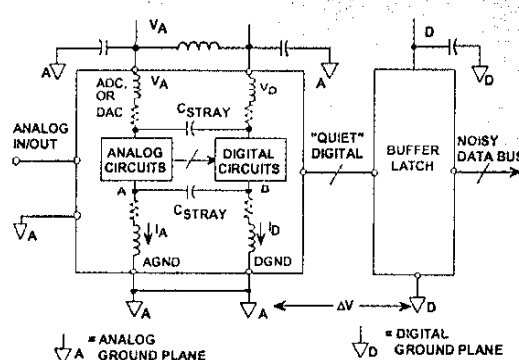
sided board should have one side dedicated to ground and the other side for interconnections. In practice, this is not possible, since some of the ground plane will be removed to support signal and power crossovers as well as via holes.

Nevertheless, as much area as possible should be preserved, and at least 75 percent should remain. After completing an initial layout, the ground layer should be checked carefully to make sure there are no isolated grounds "islands." IC ground pins located in a ground island have no current return path to the ground plane.

The best way to minimize ground impedance in a mult-card system is to use another PCB as a backplane for interconnections between cards, thus providing a continuous ground plane to the mother card. The PCB connector should have at least 30 to 40 percent of its pins devoted to ground, and these pins should be connected to the ground plane on the backplane mother card. To complete the overall system grounding scheme there are two possibilities: 1. The backplane ground plane can be con-

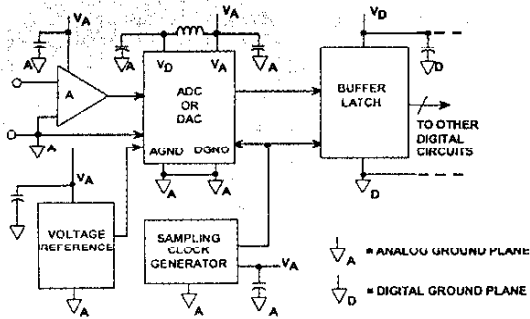


1. In order to minimize noise in high-frequency, high-speed circuits, it is essential to separate analog and digital grounds.

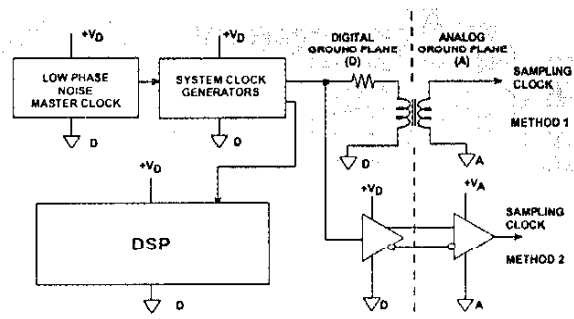


2. This diagram illustrates proper grounding of ADCs, DACs, and other mixed-signal components.

GROUND PLANE



3. This diagram shows recommended power-supply grounding and decoupling points.



4. This diagram represents the sampling-clock distribution from the DAC to the ground.

nected to chassis ground at numerous points, thereby diffusing the various ground current return paths. 2. The ground plane can be connected to a single system "star ground" point (generally at the power supply).

The first approach is often used at very-high frequencies and where the return currents are relatively constant. The low ground impedance is maintained all the way through the PCBs, the back-plane, and, ultimately, the chassis. It is critical that good electrical contact be

le where the grounds are connected to the sheet-metal chassis. This requires self-tapping sheet-metal screws or "biting" washers. Special care must be taken where anodized aluminum (Al) is used for the chassis material, since its surface acts as an insulator. In other systems, especially high-speed ones with large amounts of digital circuitry, it is highly desirable to physically separate sensitive analog components from noisy digital

components. It is usually desirable to use separate ground planes for the analog and digital circuitry. On PCBs that have analog and digital circuits, there are two separate ground planes. These planes should not overlap in order to minimize capacitive coupling between the two.

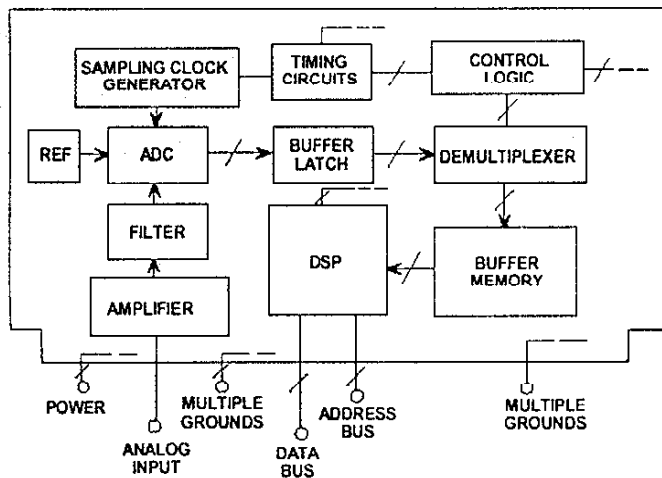
The arrangement shown in Fig. 1 illustrates that the two planes are kept separate all the way back to a common system "star" ground, generally located at the power supplies. The connections between the ground planes, the power supplies, and the "star" should be made up of multiple bus bars or wide copper braids for minimum resistance and inductance. The back-to-back Schottky diodes on each PCB are inserted to prevent accidental DC voltage from developing between the two ground systems when cards are plugged and unplugged.

Sensitive analog components, such as amplifiers and voltage references, are referenced and decoupled to the analog

ground plane. The analog-to-digital converters (ADCs) and digital-to-analog (DAC) and mixed-signal ICs should be treated as analog components and also grounded and decoupled to the analog ground plane. At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually pins designated as analog ground (AGND) and digital ground (DGND). The diagram shown in Fig. 2 will help to explain this apparent dilemma.

Inside an IC that has analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 2 shows a simple model of a converter. There is nothing that the IC designer can do about the wire-bond inductance and resistance associated with connecting the pads on the chip to the package pins except to realize it is there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY} .

In addition, there is approximately 0.2 pF of unavoidable stray capacitance between every pin of the IC package. It is the IC designer's job to make the chip work despite this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the analog ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B. It will, in turn, couple more digital noise into the analog circuit through the stray capacitance. Supply pin (V_D) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead as shown in Fig. 2.



5. Good grounding techniques are demonstrated in this sample PCB layout.

GROUND PLANE

The internal digital currents of the converter will return to ground through the V_D pin decoupling capacitor (mounted as close to the converter as possible) and will not appear in the external ground circuit. It is always a good idea (as shown in Fig. 3 to place a buffer latch adjacent to the converter to isolate the converter's digital lines from any noise, which may be on the data bus.

The buffer latch and other digital cir-

cuits should be grounded and decoupled to the digital ground plane of the PCB. Any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered

from a separate analog supply, or filtered as shown in the diagram.

All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious. The sampling clock-generation circuitry should also be grounded and heavily decoupled to the analog ground plane. Phase noise on the sampling clock produces degradation in system signal-to-noise ratio (SNR).

Ideally, the sampling clock generator should be referenced to the analog ground plane in a split-ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher frequency multipurpose system clock which is generated on the digital ground plane. If it is passed between its origins on the digital ground plane to the ADC on the analog ground plane, the ground noise between the two planes adds directly to the clock and will produce excess jitter.

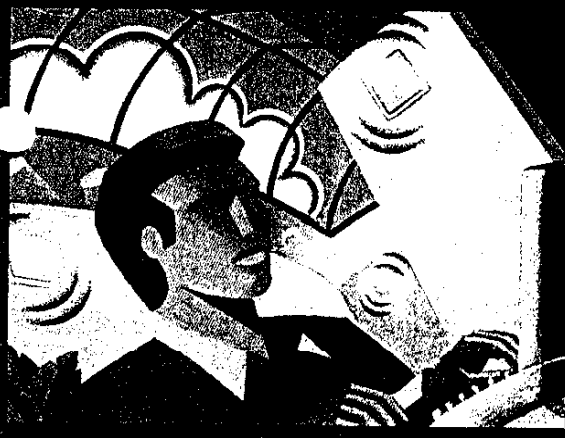
The jitter can cause degradation in the SNR and also produce unwanted harmonics. This can be remedied somewhat by transmitting the sampling-clock signal as a differential one using either a small RF transformer or a high-speed differential driver and receiver as shown in Fig. 4. The driver and receiver should be connected through emitter-coupled logic (ECL) signals to minimize phase jitter. The original master system clock should be derived from a low-phase-noise crystal oscillator.

If a ground plane is used, as it should be in most cases, it can act as a shield where sensitive signals cross. Figure 5 shows a good layout for a data-acquisition (DAQ) board where all sensitive areas are isolated from each other and signal paths are kept as short as possible.

This application note is an excerpt from the Analog Devices' 1996 text "High Speed Design Techniques," Chapter 7. *Wsp*

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